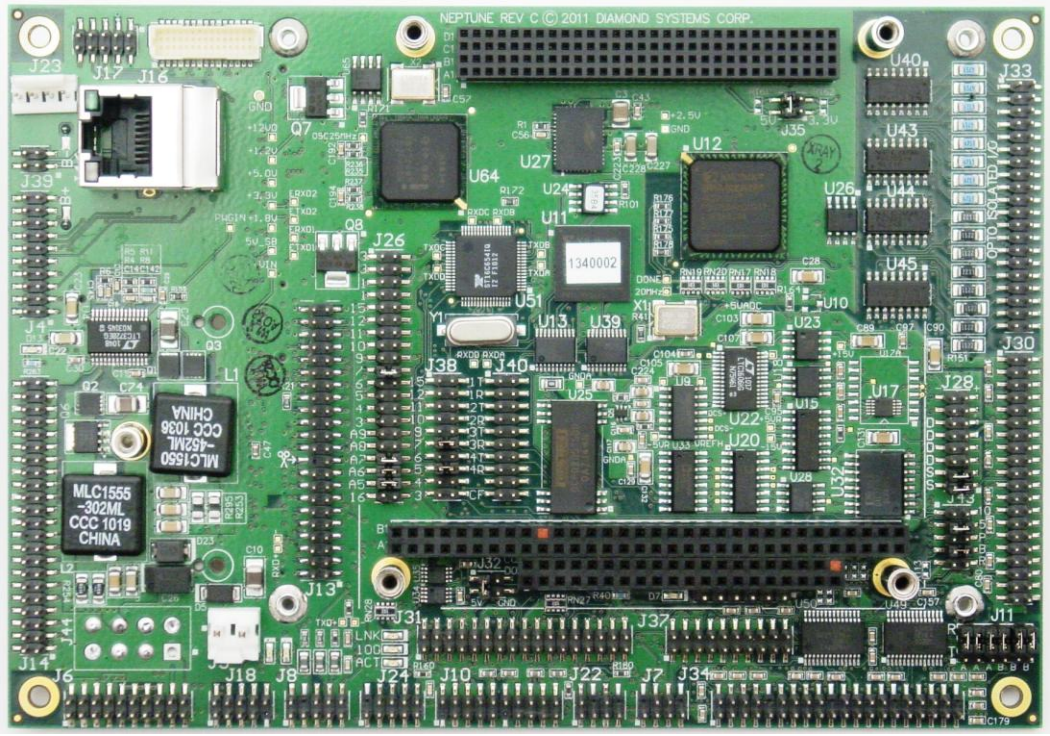
NEPTUNE Single Board Computer

EPIC Form-factor Embedded Computer with Integrated Data Acquisition and Configurable CPU



Revision	Date	Comment
1.5	9/08/2009	Initial release
2.0	5/13/14	New AMD G-Series models
2.1	5/15/15	New Intel Bay Trail E3845 models

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IMPORTANT SAFE-HANDLING INFORMATION

- **WARNING!**
- **ESD-Sensitive Electronic Equipment.**
- **Observe ESD-safe handling procedures when working with this product.**
- **Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.**
- **Always store this product in ESD-protective packaging when not in use.**

Safe Handling Precautions

Neptune contains numerous I/O connectors that connect to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage — This type of damage is almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board simply stops working because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage — On some boards, we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However, these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However, our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards — Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply. In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Board not installed properly in PC/104 stack — A common error is to install a PC/104 board accidentally shifted by 1 row or 1 column. If the board is installed incorrectly, it is possible for power and ground signals on the bus to make contact with the wrong pins on the board, which can damage the board. For example, this can damage components attached to the data bus, because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input — If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output — If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line — The digital circuitry can be damaged if a digital I/O signal is connected to a voltage above the Neptune's maximum specified voltage. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit.

Bent connector pins — This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. The most common cause of bent connector pins is when a PC/104 board is pulled off the stack by rocking it back and forth left to right, from one end of the connector to the other. As the board is rocked back and forth it pulls out suddenly, and the pins at the end get bent significantly. The same situation can occur when pulling a ribbon cable off of a pin header. If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

1. INTRODUCTION

Neptune introduces a new concept in small form-factor, board-level embedded computing.

Neptune's core embedded-PC functionality is implemented with an ETX CPU module mounted on the bottom side of an I/O baseboard. This approach results in several benefits including enhanced thermal management, increased space for I/O functions and interface connectors, and scalable processing power. Accordingly, Neptune integrates the equivalent functions of up to six embedded boards — CPU, system I/O, industry-leading data acquisition, gigabit Ethernet, and a wide-input DC-to-DC power supply — all within the compact and modularly-expandable EPIC single board computer form-factor.

Thanks to Neptune's modular architecture, you can select from a wide range of ETX-based CPUs to meet each application's specific performance, power, and cost requirements. Available processors include two of the AMD Fusion G-Series CPUs, the T56N and T40N. What's more, Neptune's on-board PC/104-*Plus* stack location facilitates the addition of both custom and off-the-shelf ISA- and PCI-interfaced expansion modules, to tune system functionality to the application's precise requirements.

Neptune is offered in a range of models that vary according to the choice of ETX CPU Module, on-board SO-DIMM SDRAM capacity, +5V input or variable-input DC/DC supply, and choice of operating temperature.

1.1 Key Features

Neptune's extensive set of features derives from functions present on the Neptune baseboard plus additional functions provided by the attached ETX computer-on-module (COM) macrocomponent. Both are summarized below.

1.1.1 ETX Computer-on-Module (COM) Features

- Processor: Choice of Intel Bay Trail E3845 CPU, AMD Fusion G-Series G-T56N or G-T40N CPUs
- RAM: 200-pin SO-DIMM socket; supports up to 8GB DDR3 SDRAM
- Graphics:
  - VGA CRT interface
  - LCD flat panel interface (LVDS); provides LCD backlight control signals
  - SDVO interface (connector directly on ETX COM, when available)
- Audio: AC'97 CODEC; mic in, line in/out signals
- 1 IDE interface; support two devices (Master/Slave) in PIO or UDMA mode
- 2 SATA ports, supporting one device each (interface connectors directly on ETX COM)
- Ethernet interface: 1 10/100Mbps port (magnetic provided on baseboard)
- 2 serial ports, supporting TTL or RS-232 signaling (signal buffers and mode selection provided on baseboard)
- Keyboard/mouse: PS/2; USB keyboard/mouse also supported
- USB: 4 USB 2.0 ports
- Other: SMbus, IrDA serial interfaces; PC speaker output; watchdog timer
- Dual system expansion buses: 16-bit ISA and 32-bit PCI
- ETX 3.0 compliant form-factor (physical and electrical)

> ***Note:*** *The ETX COM features listed below are typical. Refer to the appropriate ETX CPU module's user manual for detailed specifications.*

1.1.2 Neptune Baseboard Features

- Additional Ethernet interface: 10/100/1000Base-T port with RJ-45 connector
- 4 additional serial ports:
  - 2 RS-232/422/485
  - 2 TTL/RS-232
- Industry-leading data acquisition subsystem:
  - 32 16-bit A/D inputs usable as: 32 single-ended / 16 differential / 16 SE + 8 DI
  - 4 12-bit D/A channels
  - 2 programmable counter/timers
  - 24 programmable bidirectional digital I/O lines with 5V logic
  - 8 optoisolated digital inputs and outputs
- EEPROM configuration data storage for instant availability on power-up
- Status LEDs:
  - Power LED
  - Ethernet link and speed LEDs
- ATX-style power input and control
- On-board RTC backup battery and connector for external battery
- ETX COM socket on bottom; conforms to ETX v3.0 specification
- I/O connectors provided for all I/O
- Solid State Disk:
  - On-board CompactFlash I/II socket
  - Mounting position for optional IDE FlashDisk
- On-board PC/104-*Plus* socket; supports ISA and PCI expansion buses
- Optional Built-in DC/DC power supply:
  - Input voltage: +5V or +8V to +28V DC
  - Power consumption: 2.5W, without ETX module
  - Output power: maximum 45W, total
  - Output voltages: +5V, +3.3V (on PCI bus)
  - Switched outputs: +5V, +12V, +3.3V
- Operating temperature: up to -40°C to +85°C (depends on ETX COM)
- Operating humidity: 5% to 95% non-condensing
- Form-factor:
  - 4.53 x 6.50 inches (115mm x 165mm)
  - EPIC SBC dimensions and mounting holes

1.2 Software Compatibility

Neptune's operating system compatibility depends on both the Neptune baseboard and the specific ETX CPU module attached to it. The baseboard has been qualified for use with the following operating systems:

- Windows XP, Windows XP Embedded SP2
- Linux v2.6.23

The operating systems supported by the ETX CPU module vary according to the specific ETX module used. Consult the appropriate ETX CPU module's user manual for details on its OS (operating system) support.

1.3 Thermal Considerations and Heatspreader

All models of Neptune are specified for an operating temperature range of either -20°C to +71°C or -40°C to +85°C depending on which ETX CPU module is selected. Diamond Systems provides a heatspreader attached to Neptune as a conductive cooled thermal layer. However, this heatspreader by itself does not constitute the complete thermal solution necessary for any specific implementation, but provides a common interface between the single board computer and the customer's implementation-specific thermal solution.

The outside surface of the Neptune heatspreader must be kept at a temperature not to exceed +71°C or +85°C, again depending on the COM module. If your environment causes the temperature on the outside surface of the heatspreader to exceed the appropriate temperature, you are responsible for removing the additional heat from the system through either an additional passive thermal solution or fan solution.

Neptune's integrated heatspreader makes thermal contact with the heat generating components and provides a flat surface on the bottom of the assembly for mating to the system enclosure. This technique facilitates efficient removal of heat from the COM module without the need for a fan. Four mounting holes on the bottom of the conduction cooled heatspreader are provided to mount Neptune in an enclosure or to a bulkhead. These mounting holes are #6-32 threaded holes on 2.8" centers.

1.4 Panel I/O Board Option

The ETX module's I/O signals are available on header connectors along the edges of the Neptune baseboard. A Panel I/O Board is available that plugs into the Neptune baseboard and routes these to standard PC-style peripheral interface connectors.

2. FUNCTIONAL OVERVIEW

2.1 Block Diagrams

Figure 1 shows Neptune's functional blocks, including circuitry contained on both the Neptune baseboard and the ETX CPU module. As indicated in the block diagram, the baseboard circuitry primarily comprises the data acquisition subsystem, gigabit Ethernet controller, DC/DC power supply, and I/O interfaces, while the ETX module integrates the system's core embedded PC functionality. Although ETX CPU module processors and precise functions vary between specific modules, the block diagram of a typical ETX CPU module is shown in Figure 2.

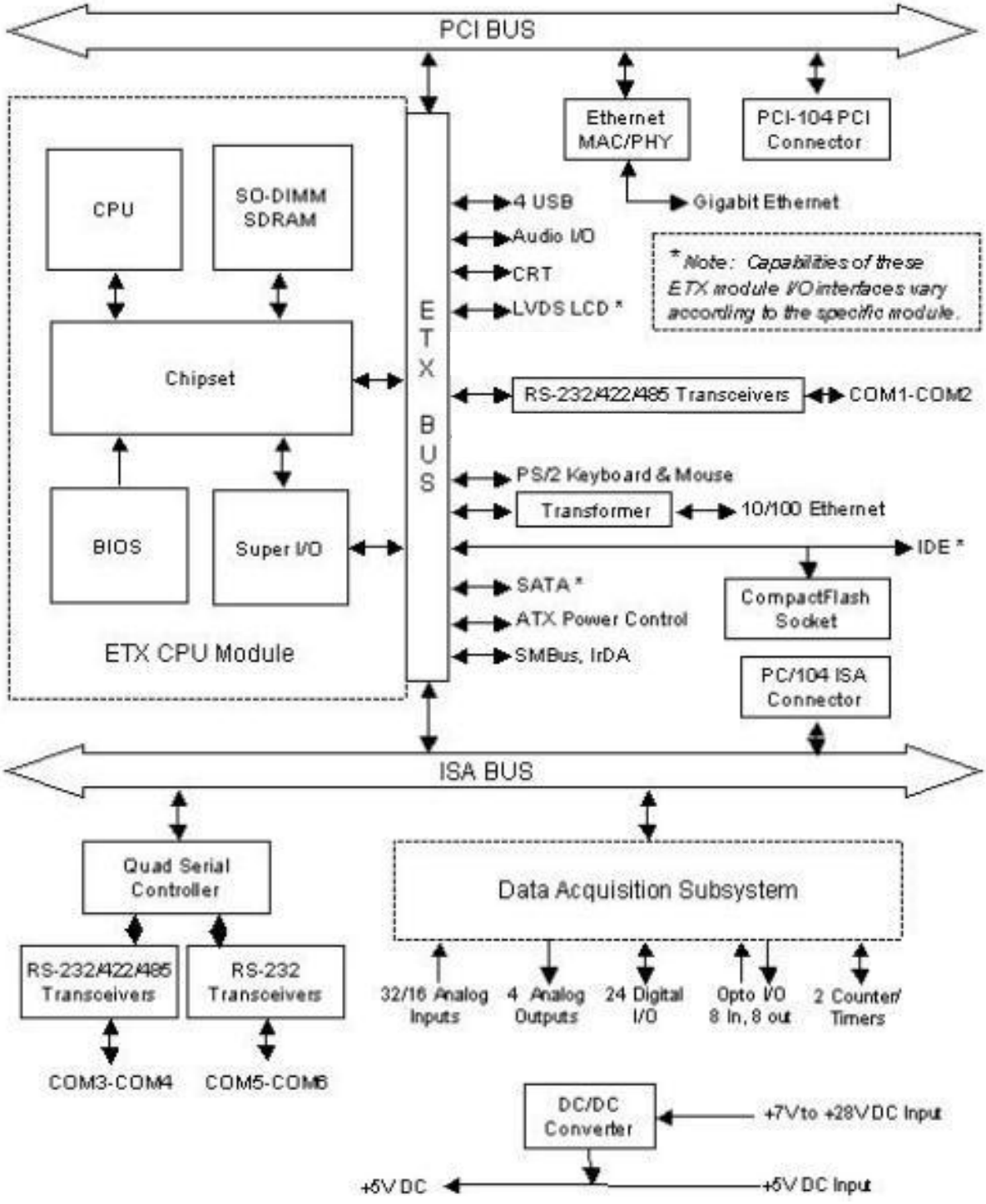


Figure 1: Neptune Baseboard Functional Block Diagram

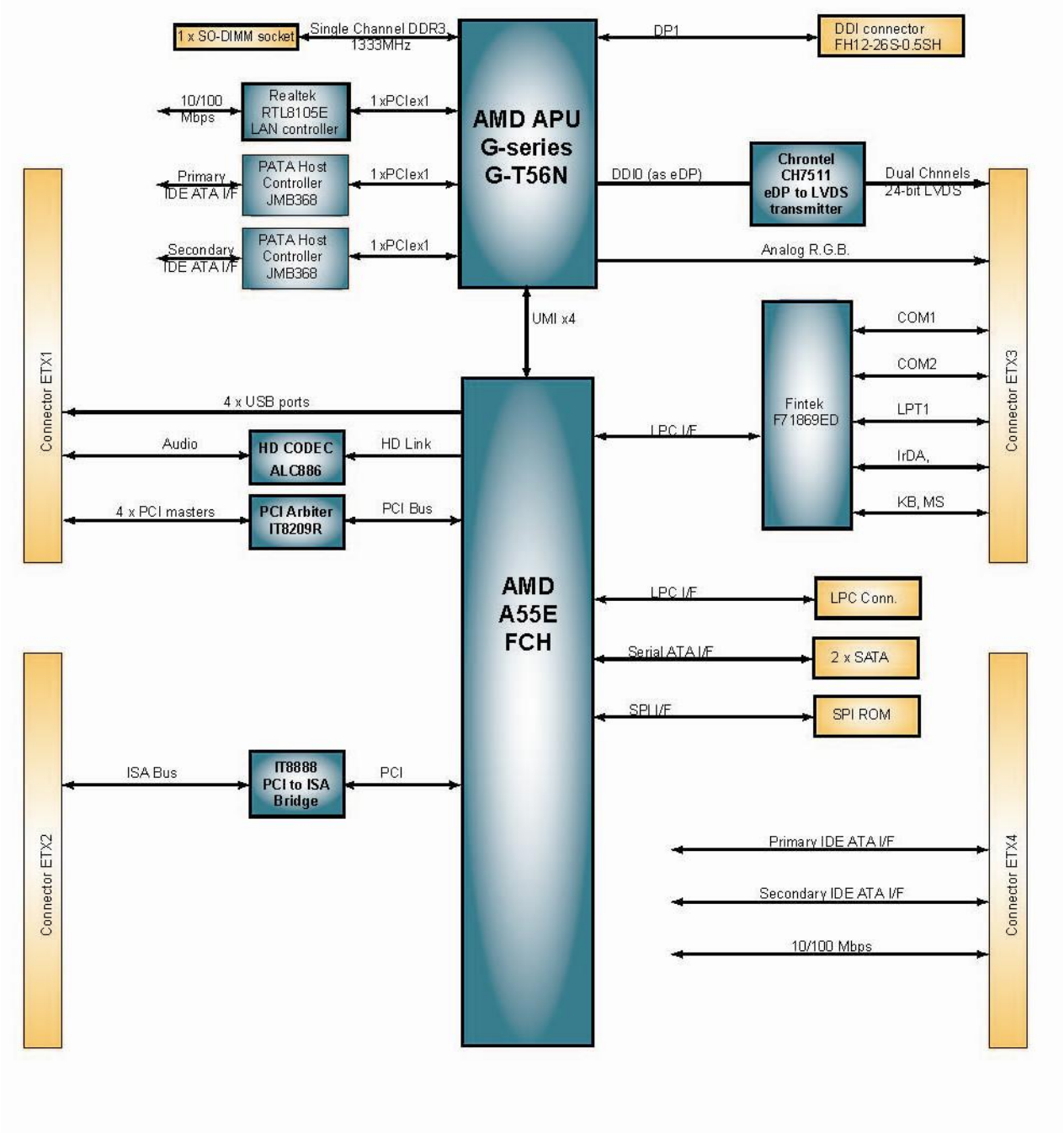


Figure 2: Typical ETX CPU Module Functional Block Diagram

2.2 Board Diagrams

Figures 3 and 4 illustrate the location of connectors and jumpers on the top and bottom side of the Neptune baseboard. The ETX CPU module attaches on the baseboard's bottom side, as indicated in Figure 3.

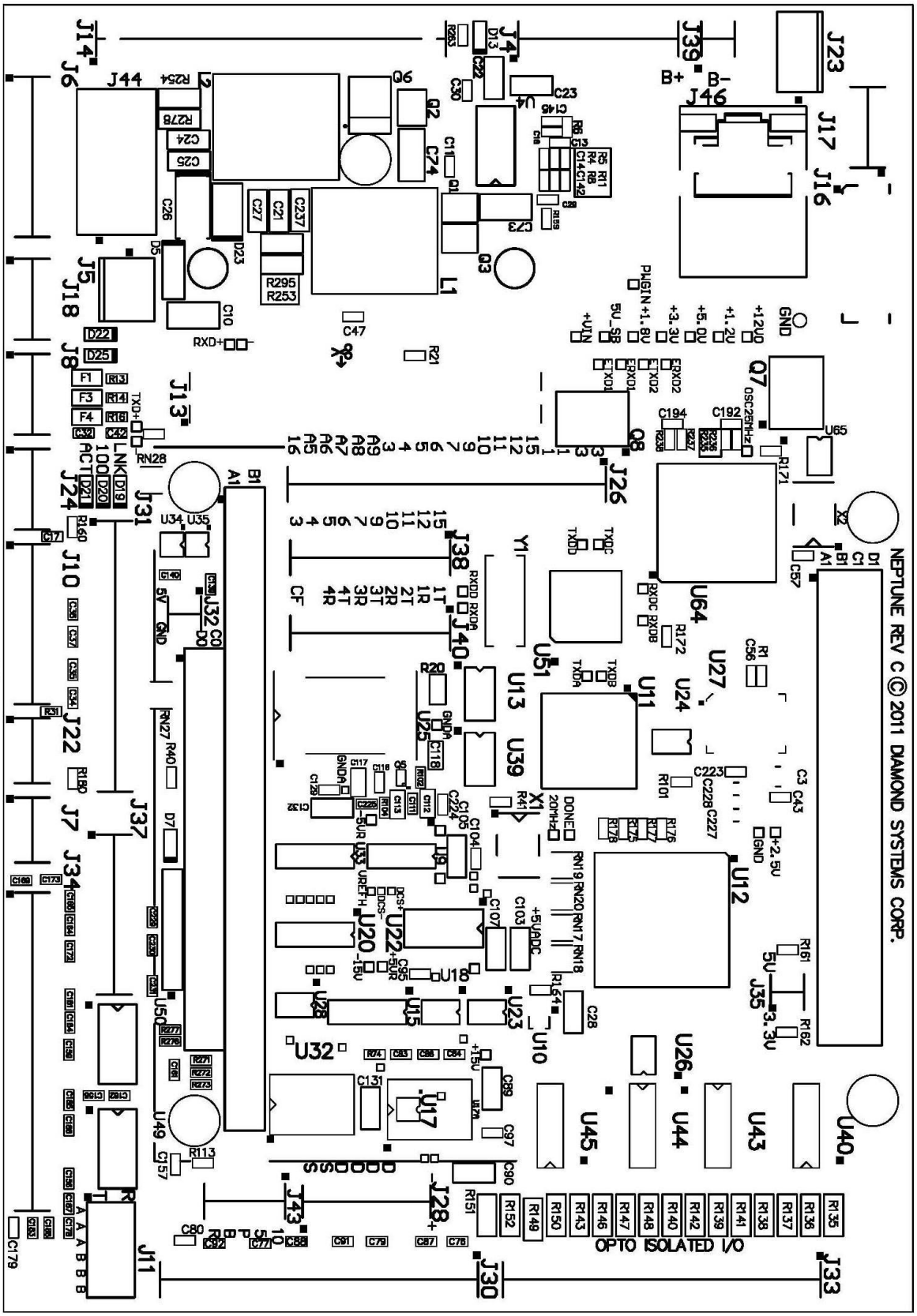


Figure 3: Neptune Top View

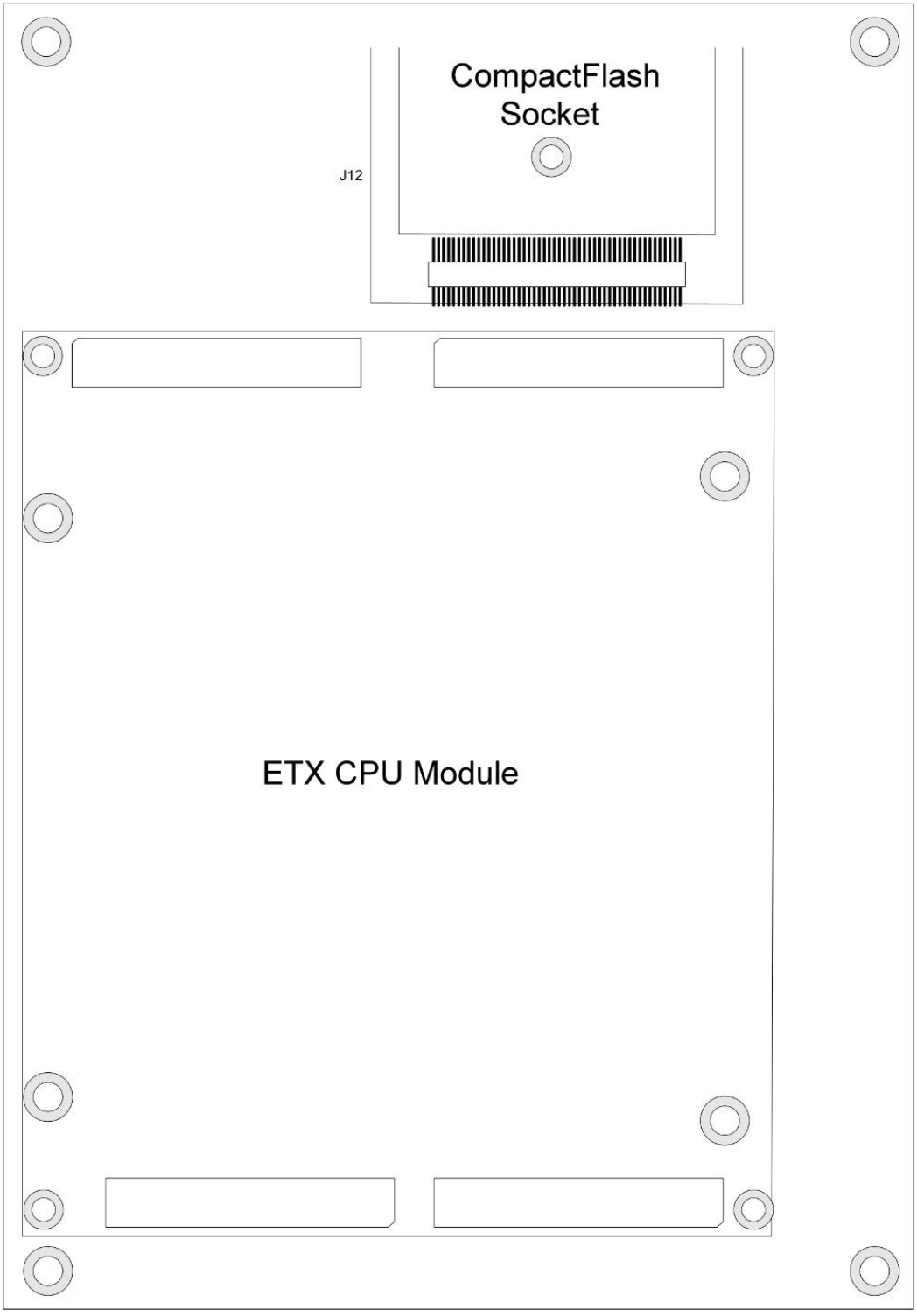


Figure 4: Neptune Bottom View

2.3 Interface Connector Summary

The table below summarizes the functions of Neptune's interface, utility, and power connectors. The table also identifies which major subsystem — ETX CPU module or Neptune baseboard — provides the electronics associated with each connector.

The table indicates which connectors mate with the optional Neptune Panel I/O Board (discussed elsewhere in this section), which provides standard PC-style I/O connectors. Alternatively, Diamond offers an optional Neptune Cable Kit (discussed in Section 5), which provides mating cable assemblies for most of Neptune's I/O interface connectors.

Signal functions relating to all of Neptune's interfaces connectors are discussed in greater detail in Section 6.

Interface Function	*Connector Designation*	*Associated Subsystem*	*Supported by Panel I/O Board?*	*Supported by Cable Kit?*
PC/104-*Plus* ISA Bus	J1, J2	ETX CPU module	n/a	n/a
PC/104-*Plus* PCI Bus	J3	ETX CPU module	n/a	n/a
ETX Utility	J4	ETX CPU module	No	Yes
Variable Input Power	J5	Neptune baseboard	No	Yes
Panel I/O Board Input Power	J6	Neptune baseboard	No	No
Keyboard and Mouse Ports	J7	ETX CPU module	Yes	Yes
VGA Display	J8	ETX CPU module	Yes	Yes
USB 2.0	J10	ETX CPU module	Yes	Yes
CompactFlash	J12	ETX CPU module	No	n/a
IDE (Primary)	J13, J14	ETX CPU module	No	Yes
LCD LVDS Interface	J16	ETX CPU module	No	No
LCD LVDS Control	J17	Neptune baseboard	No	No
Audio	J18	ETX CPU module	Yes	Yes
Utility	J22	Neptune baseboard	No	Yes
HDD Power	J23	Neptune baseboard	No	Yes
ETX Ethernet	J24	ETX CPU module	Yes	Yes
Analog I/O	J30	Neptune baseboard	No	Yes
Digital I/O	J31	Neptune baseboard	No	Yes
Optoisolated I/O	J33	Neptune baseboard	No	Yes
COM1-COM4	J34	Neptune baseboard	No	Yes
COM5-COM6	J37	ETX CPU module	Yes	Yes
Gigabit LED Connector	J39	Neptune baseboard	No	No
ATX-style Input Power	J44	Neptune baseboard	No	Yes
Gigabit Ethernet	T1	Neptune baseboard	No	No
SATA interfaces	SATA1, SATA2	ETX CPU module	No	No
Serial Digital Video Output	SDVO	ETX CPU module	No	No

Note: *ETX COM I/O functions vary according to the specific ETX module that is attached to the Neptune baseboard. For further details on functions listed above that are generated by the ETX CPU module, consult the specific ETX CPU module's user manual. SATA1/SATA2 and SDVO, when available, are supported by connectors directly on the ETX module.*

2.4 Configuration Jumper Summary

The Neptune baseboard's configuration jumper blocks are listed below. Details regarding the use of these jumpers appear in Section 5 of this document.

Jumper	*Description*
J11	Serial I/O TTL/RS-232 Selection
J26	DMA / IRQ / Address Bus Configuration
J28	Single-ended / Differential Selection
J32	DIO Pull-up/Pull-down Selection
J35	PCI Voltage selection
J38	IRQ Selection
J40	COM1-4 / CF Configuration
J43	DAC Configuration

3. GETTING STARTED

First-time Neptune users normally receive the product as part of Diamond's Neptune Development Kit, which provides everything needed to ensure rapid application development. This section of the Neptune User Manual covers basic hardware setup, power connection, system boot-up, and initial software configuration. After Neptune is up and running, refer to the later sections of this manual for the detailed hardware and software reference information needed to adapt the product to specific applications.

This section begins with a simple series of quick-start steps for rapidly bringing up Neptune and verifying its proper operation. The steps provided assume the use of Diamond's Neptune Development Kit.

The Neptune quick-start process basically consists of the following steps:

1. Install the Diamond IDE FlashDisk Drive with bootable Linux binary on the primary IDE connector.
2. Install the Neptune Panel I/O Board on its mating connectors.
3. Connect a VGA monitor.
4. Connect PS/2- or USB-based keyboard and mouse peripherals.
5. Connect the Neptune AC Adapter to the Neptune baseboard's power connector.
6. Turn on the monitor and plug in the AC Adapter.
7. At this point, Neptune should boot-up to a Linux prompt.

The above steps will be discussed in detail, after the brief overview of the Neptune Development Kit and its contents that follows.

Important Safe-Handling Information

WARNING: ESD-Sensitive Electronic Equipment!

Observe ESD-safe handling procedures when working with this product.

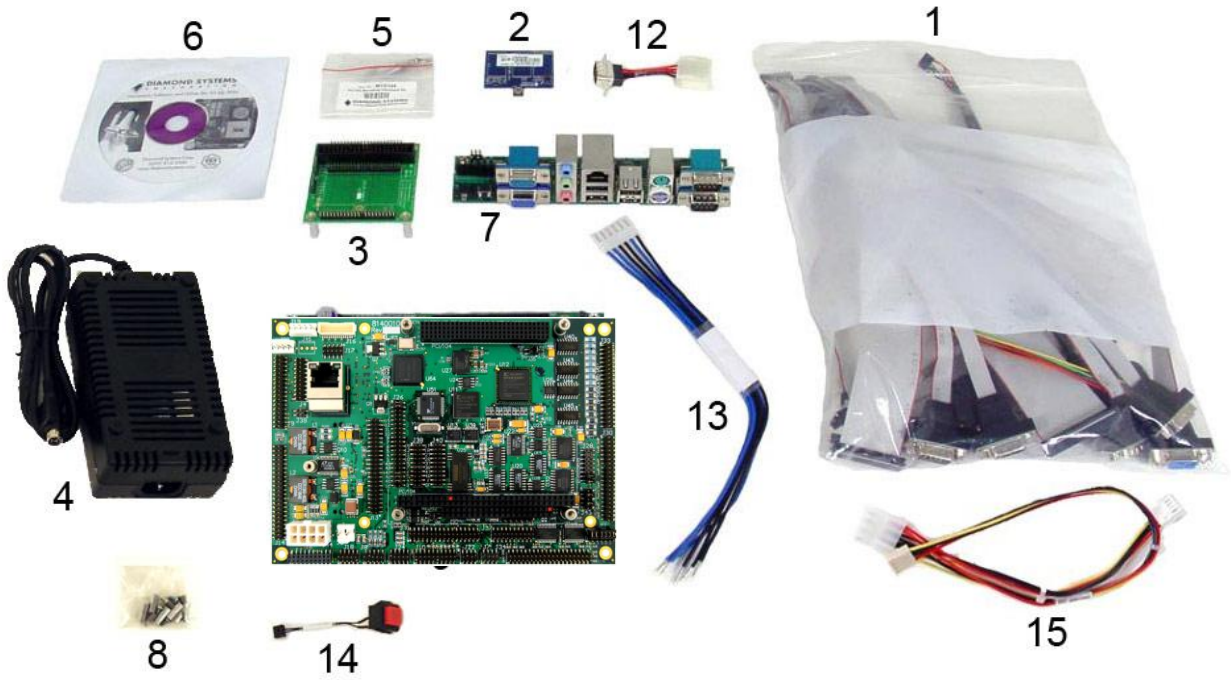
Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Please refer to page 5 of this manual ("Important Safe-Handling Information") for further details.

3.1 Introducing the Neptune Development Kit

The Neptune Development Kit provides everything required for Neptune-based rapid application development. The photos and table below identify the boards, cables, and other items included in the kit.

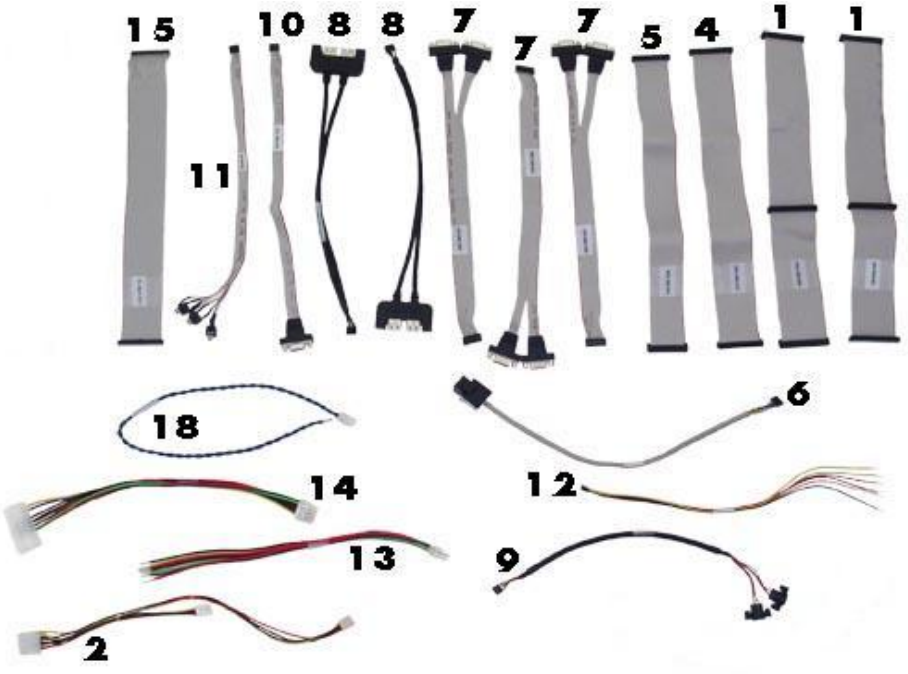


The fifteen Neptune Development Kit items pictured above are identified below.

Item	*Diamond P/N*	*Description*
1	C-NPT-KIT	Neptune Cable Kit
2	DK-LNX-NPT	512MB FlashDisk with bootable Linux, CD
3	ACC-IDEEXT	FlashDisk Programmer Board (includes 40- and 44-pin IDE cables)
4	PS-5V-04	AC Adapter (100-240VAC in, 5VDC @ 8A out)
5	6810041	Neptune Panel I/O Board mounting hardware (not shown)
6	6710010	Neptune software and documentation CD
7	PNL-NPT-01	Neptune Panel I/O Board
8	MTG104	PC/104 Mounting Hardware
9	NPT-xxxx-xxx	Neptune SBC (model number varies according to which Development Kit was ordered)
12	6981093	Transition cable for power interface between AC Adapter and Panel I/O Board
13	6981092	Cable for power interface between Panel I/O Board and optional PC/104 power supply module
14	6981094	Power button interface to Panel I/O Board Utility connector
15	6981006	Auxiliary power interface for 40-pin IDE devices (CD-ROM)

3.1.1 Neptune Cable Kit

The Neptune cable kit (part number C-NPT-KIT) provides convenient access to all of Neptune's I/O features. The kit's cables are shown in the photo below and are identified in the table that follows.

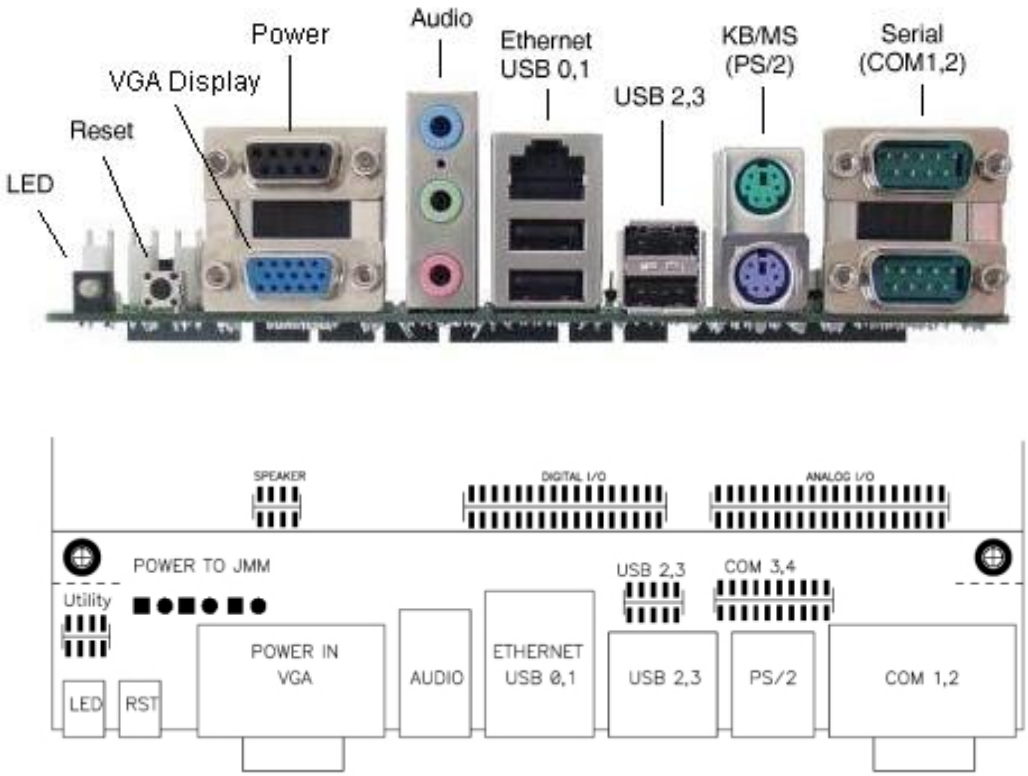


The components of the Neptune Cable Kit are listed below.

Item	*Qty*	*Diamond P/N*	*Description*	*Connects to…*
1	2	6981004	IDE (44-pin)	J13, 14
2	1	6981006	Power output	
4	1	6981072	Analog I/O	J30
5	1	6981073	Digital I/O	J31
6	1	6981080	100Mbit Ethernet	J24
7	3	6981081	Dual serial	J34, J37
8	2	6981082	Dual USB	J10
9	1	6981083	Keyboard/Mouse	J7
10	1	6981084	VGA out	J8
11	1	6981085	Audio I/O	J18
12	1	6981088	Baseboard utility signals	J4
13	1	6981090	Power input cable	J5
14	1	6981091	ATX-style input power	J44
15	1	6981141	Optically isolated I/O	J33
18	1	6981144	Variable DC input power	J5

3.1.2 Neptune Panel I/O Board

The Neptune Panel I/O Board mates with the bank of connectors located along the side of the Neptune baseboard, as shown in the figures below. The board provides standard connector access for many of Neptune's PC-style interfaces, a reset button, and a power LED.



Neptune Panel I/O Board, Front and Top views

3.1.3 512MB Flashdisk with Linux

The Neptune Development Kit contains a 512MB IDE solid-state flashdisk preformatted with Diamond's compact, quick-boot Linux OS based on a 2.6.x kernel. The Linux system utilizes the Minix file system for enhanced file protection during power loss or improper shutdown, and Grub bootloader for boot-up. In addition to the Linux OS, the flashdisk image includes Diamond's Universal Driver, which supports the Neptune baseboard's data acquisition functions.

A binary image of contents of the flashdisk device is also included in the Neptune Software Development Kit. This image may be used for preparing additional Neptune-based systems for operation. A Neptune Linux Software Development Kit (SDK), which includes OS source code along with a complete development toolchain, is also available (contact Diamond for further details).

3.1.4 Flashdisk Programmer Board

The flashdisk Programmer Board allows a flashdisk and an external IDE drive to share the Neptune baseboard's primary IDE connector (J13). In this case, the flashdisk and external device are used as Master and Slave IDE devices, respectively. The flashdisk Programmer Board provides the flexibility of interfacing to external drives requiring either 40- or 44-pin IDE cables.

The flashdisk Programmer Board is not required on Neptune configurations with ETX CPU modules that provide a secondary IDE channel; in this case, an external IDE device can be connected to the baseboard's secondary IDE connector (J14). In addition, on Neptune assemblies whose ETX CPU module has built-in SATA connector(s), a SATA-interfaced drive can be used in lieu of an IDE drive attached to a flashdisk Programmer Board.

3.1.5 AC Adapter

An AC Adapter (P/N PS-5V-04), included in the Neptune Development Kit, converts a 110VAC to 240VAC power source to 5VDC suitable for powering a Neptune SBC. The AC Adapter's power output cable is equipped with a connector that mates with the Neptune baseboard's ATX-style input power connector (J44).

> ***Note:*** *There are numerous ways to power a Neptune-based system — according to the power source and its voltage, whether the application requires instant-on access or use of a power switch (or button), and whether ATX-style soft shutdown is required.*

3.1.6 Miscellaneous Cables

Three additional special-function cables are included in the Neptune Development Kit:

- 6981092 — Used when the Panel I/O Board is present along with a wide-voltage PC/104 Power Supply module, such as Diamond's Jupiter MM. This routes incoming power from the Panel I/O Board to the PC/104 Power Supply module. This cable is included in Panel I/O Board Kit.
- 6981093 — Connects between the AC Adapter (PS-5V-04) and the DB9 power input connector on the Panel I/O Board. Allows the use of the AC Adapter when Neptune and a Panel I/O Board are mounted within an enclosure such as Diamond's Triton. This cable is included in Panel I/O Board Kit.
- 6981006 — Provides power from the Neptune board to an IDE device having a 40-pin interface.

3.1.7 Software and Documentation CD

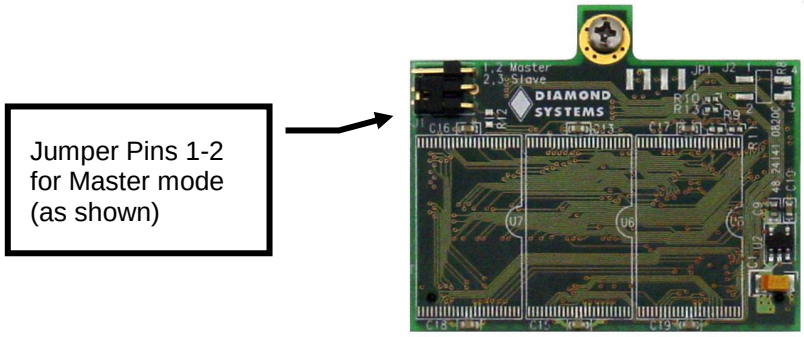
The Neptune Development Kit also includes a Software and Documentation CD, which contains Neptune documentation (including this manual) and support software. The CD provides drivers specific to the Neptune baseboard and its attached ETX CPU module, for operation under Windows XP, Windows XP Embedded, and Linux. The CD also contains Diamond's Universal Driver Software, which supports the analog and digital I/O capabilities of the Neptune baseboard, including binaries and full documentation.

3.2 System Setup

3.2.1 Installing the Flashdisk

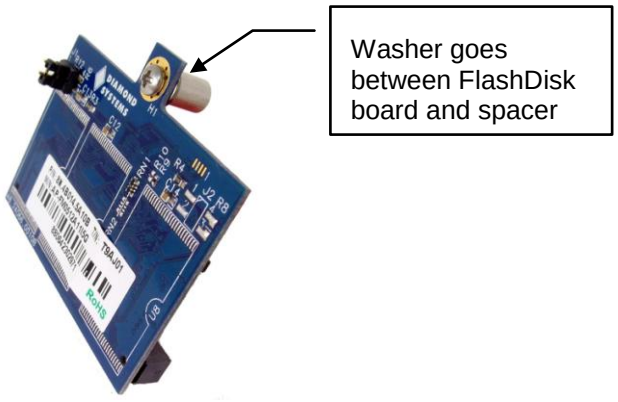
The flashdisk module installs directly on the Neptune baseboard's primary IDE connector (J13) and attaches via a spacer and two screws to a mounting hole on the baseboard. Mounting hardware is provided in the Neptune Development Kit in the packet marked with DSC# 6801008. Use the following installation procedure:

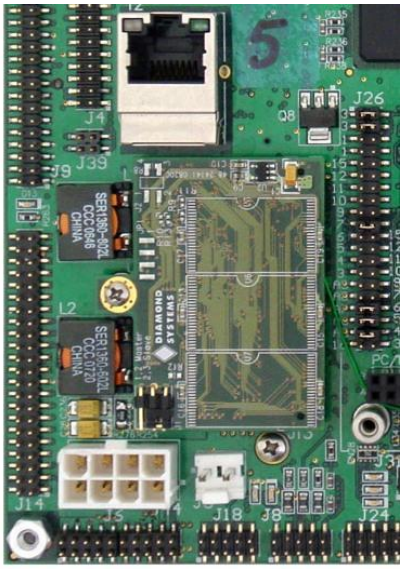
1. To ensure that Neptune boots directly from the flashdisk, place the jumper block over pins 1–2. This configures the flashdisk as an IDE Master device. See the figure below.



2. Connect round spacer DSC# 6841002 to the flashdisk module using one 2-56x pan head screw and one #2 flat washer. The spacer should be on the side of the flashdisk module with the female IDE connector. The washer should be on the top of the spacer. See the figure below.
3. Attach the female IDE connector on the flashdisk to the IDE connector J13 on the Neptune board.
4. Fasten the flashdisk in place by inserting one 2-56x pan head screw from the solder side of the Neptune board into the round spacer.

The figure below shows the Neptune baseboard with the flashdisk attached.





3.2.2 Installing the Neptune Panel I/O Board

Install the Neptune Panel I/O Board on the Neptune baseboard as follows, using the Panel I/O Board Mounting Hardware Kit (part number 6810041) provided in the Neptune Development Kit:

1. Carefully mate the Panel I/O Board with the set of eight 2 mm pin-header connectors located on the edge of the Neptune board, as shown in the figures below.
2. Screw a pan head Phillips 4-40 screw through each of the two mounting holes from the top (component side) of the Panel I/O Board into the 7 mm round spacer provided on the top of the Neptune board.

3.2.3 Connecting display, keyboard, and mouse peripherals

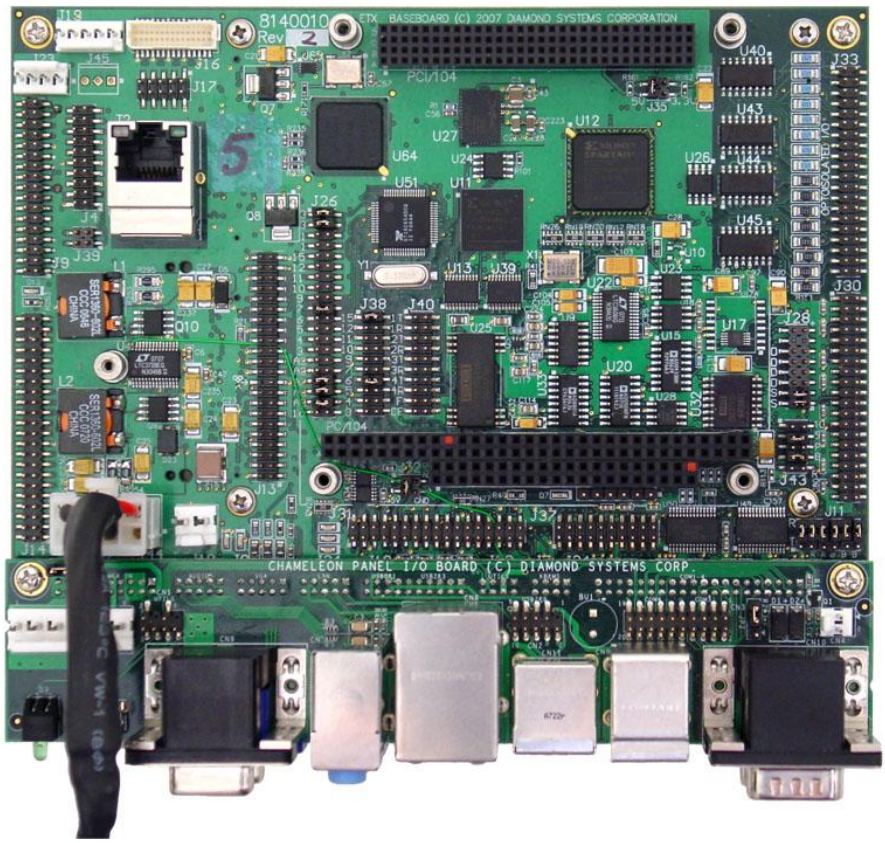
Neptune provides both VGA monitor and LVDS flat panel display interfaces. Recognizing the complexities associated with connection to parallel-interfaced flat panels, this quick-start process assumes the use of a standard VGA-compatible monitor (LCD or CRT). Connect a VGA-compatible display to the female DB15 connector on the Panel I/O Board.

The Neptune SBC supports either PS/2- or USB-based keyboard and mouse devices. Connect these devices to the corresponding connectors on the Panel I/O Board.

> ***Note:*** *a mouse is not required for basic operation of the Neptune-based system when booting from the flashdisk's quick-boot Linux OS.*

3.2.4 Connecting Power

Connect the power output cable from the AC Adapter (P/N PS-5V-04) to its mating connector (J44) on the Neptune baseboard. At this point — with the flashdisk, Panel I/O Board, and AC Adapter installed as described above — your Neptune setup should appear as shown below.



Neptune with Panel I/O Board and power cable installed

3.3 Booting the System

Plug in and turn on the VGA video display. Then, attach the power cord to the PS-5V-04 AC Adapter, and plug the power cord into an AC power outlet.

Neptune should power up immediately, displaying information regarding the BIOS and Diamond Linux followed by a system prompt.

3.4 Demonstrating Data Acquisition Operation

The Linux installed on the flashdisk contains software demonstration programs for Neptune's data acquisition features. You may access the directory of these programs by typing:

```
>cd /home/NEPTUNE
```

The source code, makefile, and executables of the demonstration programs reside in this directory. Each demonstration program executable (and its source code) appears in its own directory. A good first demonstration program to run is the DSCADAutoCal program.

The DSCADAutocal program will calibrate the Neptune baseboard's A/D data acquisition circuitry to guarantee accurate A/D input readings. To run the program type the following while in the demonstration programs directory:

```
>./DSCADAutoCal/DSCADAutoCal
```

The program will ask you to input the following values:

- Base address: This is the base address of the board determined by jumper settings on J26, see page 55 for more details. For demonstration purposes type 0x300.
- Range to calibrate: This is the A/D modes users would typically calibrate. The modes are 0-3, 8-15. For demonstration purposes type 255.
- Range to boot: This is the A/D mode users typically boot up the board in. The modes are 0-3, 8-15. For demonstration purposes type 0.

Once initiated, the program will calibrate the mode the user specified. The process may take up to 15 seconds, after which the error values will be printed on screen for each mode; values less than +-2 are within tolerance.

For more details regarding A/D modes refer to section "Input Ranges and Resolutions" in the data acquisition sections of this document. For more information regarding the data acquisition software API and functions please refer to the Diamond Systems Universal Driver software manual located here.

3.5 Additional System Configuration

3.5.1 BIOS Setup

The Neptune ETX CPU module's BIOS ROM provides a wide range of configuration options. When you power up Neptune, you can immediately enter the BIOS "Setup" utility (prior to OS boot-up) in order to adjust BIOS settings to match your system's peripheral devices and other requirements, and to configure various other hardware and software parameters.

Options configurable via Setup typically include:

- Number and type of mass storage devices
- Boot device priority
- Video display type and resolution
- IDE, serial, and parallel interface modes and protocols
- PCI and PnP configuration
- Power management setup
- Automatic power-up after LAN connection, RTC alarm, power resumption, etc.
- System monitoring and security functions

The precise configuration options available via the BIOS Setup utility — and the specific keystroke sequence required to launch Setup on power-up — vary according to the specific ETX CPU module attached to the Neptune Baseboard. Refer to the ETX CPU module's user manual for further details.

3.5.2 Operating System Drivers

Depending on the operating system to be installed on your Neptune setup, it may be necessary to install software drivers for on-board interface controllers. The driver requirements (if any) will depend on both the Neptune Baseboard and the attached ETX CPU module. Drivers for Windows XP and Linux 2.6, if required, are included on the Software and Documentation CD that is included in the Neptune Development Kit. This software is also available for download from Diamond's website.

3.5.3 Using a Hard Drive, CD-ROM, or other IDE device along with the FlashDisk

There are several ways to attach additional devices such as hard drives and CD-ROM drives to the Neptune system, while continuing to use the provided flashdisk as a primary boot device:

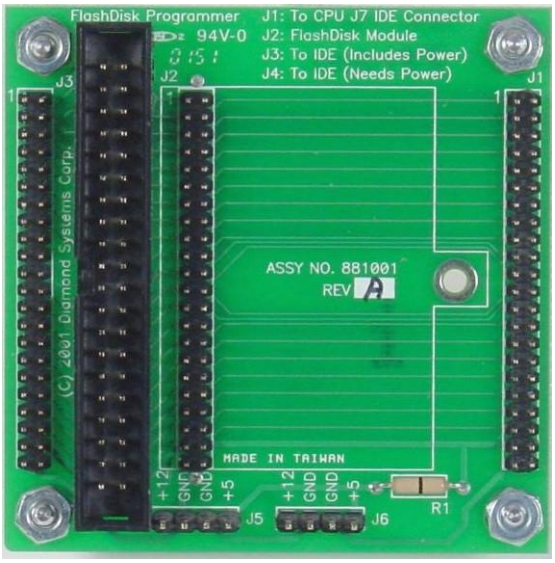
1. Attach a second IDE device to the primary IDE interface using the flashdisk Programmer Board to provide a simultaneous connection of both the flashdisk module and the IDE device. Instructions are provided below regarding installation and use of the flashdisk Programmer Board.
2. In Neptune configurations with an ETX CPU module that includes one or two SATA interfaces, you can connect a SATA hard drive directly to a SATA connector on the ETX module using a standard internal SATA cable (generally available with the drive).

3.5.4 Installing the Flashdisk Programmer Board

The flashdisk Programmer Board (FDPB) provided with the Neptune Development Kit enables the simultaneous connection of both a flashdisk module and a standard IDE hard drive or CD-ROM drive to the primary IDE connector on the Neptune board.

1. Install the flashdisk to the Flashdisk Programmer Board using the instructions provided earlier in this chapter.
2. Attach the female IDE connector on the flashdisk to the IDE connector (J2) on the FDPB.
3. Fasten the flashdisk in place by inserting one 2-56x pan head screw from the solder side of the FDPB board into the round spacer. The figure below shows the appearance of the Neptune board with the flashdisk attached.
4. Connect the connector J1 on the FDPB to the primary IDE connector (J13) on the Neptune baseboard using one of the 44-wire ribbon-cables (DSC# 6981004) from the Neptune Cable Kit.
5. Connect the IDE device to either the 40-pin (0.1-inch spacing) J4 connector on the FDPB or the 44-pin (2 mm spacing) J3 connector on the FDPB. Any two devices (i.e. flashdisk and HDD) may be connected simultaneously using this board with proper master / slave jumper configurations on the devices. Since the flashdisk is configured as an IDE Master, be sure to configure the added IDE device as a Slave.

Note: *The 44-pin connectors (J1, J2, and J3) and mating cables carry +5V power, but the 40-pin connector (J4) and mating cable do not. J5 and J6 on the FDPB or J13 on the Neptune may be used to provide power to an IDE device when the device is attached to the 40-pin J4 connector on the FDPB using the Auxiliary Power Cable (DSC# 6981006) provided with the Neptune Development Kit. If +12V power is required, it must be supplied externally.*



FlashDisk Programmer Board

4. INTERFACE CONNECTOR DETAILS

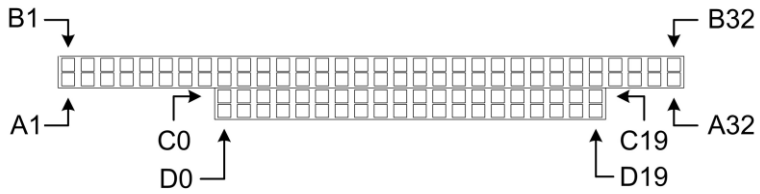
This section describes functions associated with the Neptune baseboard's PC/104-*Plus* bus expansion stack, utility, and power interface connectors in greater detail. Refer to Section 3 of this document for information regarding mating cable assemblies that are provided in the Neptune cable and Panel I/O Board kits.

4.1 PC/104-*Plus* stacking location (J1, J2, J3)

This set of three connectors accommodates the addition of either PC/104 (ISA bus only), PC/104-*Plus* (ISA and PCI buses), or PCI-104 (PCI bus only) modules on top of the Neptune baseboard. Specifications and other details on all three of these expansion module standards are available from the website of the PC/104 Consortium (http://www.pc104.org).

4.1.1 PC/104-*Plus* ISA Bus (J1, J2)

Connectors J1 (A/B) and J2 (C/D) carry the PC/104-*Plus* expansion stack location's 104-pin ISA bus signals. These signals, generated by Neptune's ETX CPU module, are essentially identical in function and signaling to those of the 16-bit PC/AT bus, except for the physical design.



A 64-pin header (J1) incorporates the 8-bit "PC bus" connector signals, while a 40-pin header (J2) incorporates the 16-bit bus connector signals. Additional grounds and keys (missing pins) have been added within the 104-pin PC/104-*Plus* ISA bus array comprised by J1 and J2.

The signal names and functions for J1 and J2 are listed in the table on the following page. The pin numbering represents the view from the top of the board.

J1 Connector

IOCHCHK-	**A1**	**B1**	GND
SD7	**A2**	**B2**	RESETDRV
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ9
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	ENDXFR-
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	Key (no pin)
AEN	**A11**	**B11**	SMEMW-
SA19	**A12**	**B12**	SMEMR-
SA18	**A13**	**B13**	IOW-
SA17	**A14**	**B14**	IOR-
SA16	**A15**	**B15**	DACK3-
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1-
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	REFRESH-
SA11	**A20**	**B20**	SYSCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2-
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	GND
GND	**A32**	**B32**	GND

J2 Connector

GND	**C0**	**D0**	GND
SBHE-	**C1**	**D1**	MEMCS16--
LA23	**C2**	**D2**	IOCS16-
LA22	**C3**	**D3**	IRQ10
LA21	**C4**	**D4**	IRQ11
LA20	**C5**	**D5**	IRQ12
LA19	**C6**	**D6**	IRQ15
LA18	**C7**	**D7**	IRQ14
LA17	**C8**	**D8**	DACK0-
MEMR-	**C9**	**D9**	DRQ0
MEMW-	**C10**	**D10**	DACK5-
SD8	**C11**	**D11**	DRQ5
SD9	**C12**	**D12**	DACK6-
SD10	**C13**	**D13**	DRQ6
SD11	**C14**	**D14**	DACK7-
SD12	**C15**	**D15**	DRQ7
SD13	**C16**	**D16**	+5
SD14	**C17**	**D17**	MASTER-
SD15	**C18**	**D18**	GND
Key (no pin)	**C19**	**D19**	GND

4.1.2 PC/104-*Plus* PCI Bus (J3)

The Neptune baseboard's PC/104-*Plus* PCI expansion bus signals are generated by the ETX CPU module, and are essentially identical in function and signaling to a normal PC motherboard's 32-bit PCI bus except for the physical connector, a 120-pin header (J3) arranged as four 30-pin rows. Several additional pins on the PC/104-*Plus* connectors implement added grounds and keys.

GND/5.0V	**A1**	**B1**	Reserved	+5V	**C1**	**D1**	AD00
VI/O	**A2**	**B2**	AD02	AD01	**C2**	**D2**	+5V
AD05	**A3**	**B3**	GND	AD04	**C3**	**D3**	AD03
CMD/BE0-	**A4**	**B4**	AD07	GND	**C4**	**D4**	AD06
GND	**A5**	**B5**	AD09	AD08	**C5**	**D5**	GND
AD11	**A6**	**B6**	VI/O	AD10	**C6**	**D6**	M66EN
AD14	**A7**	**B7**	AD13	GND	**C7**	**D7**	AD12
+3.3V	**A8**	**B8**	CMD/BE1-	AD15	**C8**	**D8**	+3.3V
SERR-	**A9**	**B9**	GND	SB0-	**C9**	**D9**	PAR
GND	**A10**	**B10**	PERR-	+3.3V	**C10**	**D10**	SDONE
STOP-	**A11**	**B11**	+3.3V	LOCK-	**C11**	**D11**	GND
+3.3V	**A12**	**B12**	TRDY-	GND	**C12**	**D12**	DEVSEL-
FRAME-	**A13**	**B13**	GND	IRDY-	**C13**	**D13**	+3.3V
GND	**A14**	**B14**	AD16	+3.3V	**C14**	**D14**	CMD/BE2-
AD18	**A15**	**B15**	+3.3V	AD17	**C15**	**D15**	GND
AD21	**A16**	**B16**	AD20	GND	**C16**	**D16**	AD19
+3.3V	**A17**	**B17**	AD23	AD22	**C17**	**D17**	+3.3V
IDSEL0	**A18**	**B18**	GND	IDSEL1	**C18**	**D18**	IDSEL2
AD24	**A19**	**B19**	CMD/BE3	VI/O	**C19**	**D19**	IDSEL3
GND	**A20**	**B20**	AD26	AD25	**C20**	**D20**	GND
AD29	**A21**	**B21**	+5V	AD28	**C21**	**D21**	AD27
+5V	**A22**	**B22**	AD30	GND	**C22**	**D22**	AD31
REQ0-	**A23**	**B23**	GND	REQ1-	**C23**	**D23**	VI/O
GND	**A24**	**B24**	REQ2-	+5V	**C24**	**D24**	GNT0-
GNT1-	**A25**	**B25**	VI/O	GNT2-	**C25**	**D25**	GND
+5V	**A26**	**B26**	CLK0	GND	**C26**	**D26**	CLK1
CLK2	**A27**	**B27**	+5V	CLK3	**C27**	**D27**	GND
GND	**A28**	**B28**	INTD-	+5V	**C28**	**D28**	RST-
+12V	**A29**	**B29**	INTA-	INTB-	**C29**	**D29**	INTC-
-12V	**A30**	**B30**	Reserved	Reserved	**C30**	**D30**	GND / 3.3V KEY

4.2 ETX Utility (J4)

The Neptune baseboard provides a 20-pin header with access to the ETX Utility signals listed in the table below.

Note: *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

BATT	1	2	GND
SMB_BTLOW-	3	4	SMB_DATA
SMB_CLK	5	6	I2_DAT
I2_CLK	7	8	JILI_DAT
JILI_CLK	9	10	GND
IRDA_TX	11	12	IRDA_RX
RSM_RST-	13	14	SMB_ALRT-
SMB_GPE1-	15	16	SMB_GPE2-
EXT_SMI-	17	18	(not used)
KB_INH	19	20	(not used)

Signal	***Definition***
BATT	3V battery input for real-time clock and non-volatile memory
SMB_BTLOW-	Battery low input; drive low to signal low battery condition or other event
SMB_CLK	System bus management clock; e.g., support for temperature/battery monitoring
SMB_GPE1-	General-purpose power management input event
SMB_DATA	System bus management data; e.g., support for temperature/battery monitoring
SMB_ALRT-	System management bus alert input; drive low to signal event on SMB
SMB_GPE2-	General-purpose power management input event
I2_CLK	No connection
I2_DAT	No connection
IRDA_RX	Infrared receive
IRDA_TX	Infrared transmit
RSM_RST-	Resume reset input; used to reset ETX module power management.
JILI_CLK	LCD panel parameter EEPROM I^2C clock
JILI_DAT	LCD panel parameter EEPROM I^2C data
EXT_SMI-	System management interrupt input; drive low to initiate interrupt event
KB_INH	Keyboard inhibit; assert to inhibit keyboard input
GND	Ground

4.3 Variable Input Power (J5)

This connector is used for connection of an external +8V to +28V DC power source. Maximum DC/DC conversion efficiency will be achieved when this voltage is close to 28V DC.

1	+VWIN
2	GND

Signal	*Definition*
+VWIN	+8 to +28V DC Input voltage
GND	Ground

4.4 Panel I/O Board Input Power (J6)

This connector provides power input from a connector located on the Neptune I/O Panel. This provides a means to power Neptune through the I/O Panel when it is packaged within an enclosure.

+5V in	**1**	**2**	+5V in
+5V in	**3**	**4**	+5V in
+5V in	**5**	**6**	+5V in
+VWIN	**7**	**8**	+VWIN
GND	**9**	**10**	GND
GND	**11**	**12**	GND
GND	**13**	**14**	GND
GND	**15**	**16**	GND
+12V in	**17**	**18**	+12V in
+5V standby	**19**	**20**	PS_ON

Signal	*Definition*
+5V in	+5V input
+12V in	+12V input
+5V standby	+5V standby power; powers board when in standby mode.
PS_ON	Power Supply ON. Feedback pin for external ATX supply, when needed; pulled low when on-board power is inactive.
+VWIN	Variable input DC power: +5 to +28 VDC
GND	Ground

Note: *Optionally, a power supply module plugged into Neptune's PC/104-*Plus *expansion stack location may be used to power the system through the power pins on the expansion module stacking bus.*

4.5 Keyboard and Mouse Ports (J7)

Connector J7 provides signals for connection of PS/2-interfaced keyboard and mouse peripherals. This connector also mates with Neptune's optional Panel I/O Board, resulting in its signals being routed to standard PC-style connectors.

Note: *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

+5V out	**1**	**2**	(not used)
Keyboard data	**3**	**4**	Mouse data
Keyboard clock	**5**	**6**	Mouse clock
GND	**7**	**8**	(not used)

Signal	***Definition***
+5V out	Switched +5V DC for powering PS/2 devices (via PS/2 connectors, pin 4)
Keyboard data	Keyboard data (via keyboard PS/2 connector, pin 1)
Mouse data	Mouse data (via mouse PS/2 connector, pin 1)
Keyboard clock	Keyboard clock (via keyboard PS/2 connector, pin 5)
Mouse clock	Mouse clock (vial mouse PS/2 connector, pin 5)
GND	Ground to PS/2 connectors, pin 3

4.6 VGA Display (J8)

Connector J8 provides signals for connecting a standard VGA monitor. This connector also mates with Neptune's optional Panel I/O Board, resulting in the VGA signals being routed to a standard PC-style connector.

Note: *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

Red	**1**	**2**	GND
Green	**3**	**4**	(not used)
Blue	**5**	**6**	GND
HSYNC	**7**	**8**	VGADAT0
VSYNC	**9**	**10**	VGACLK0

Signal	***Definition***
Red	RED signal (positive, 0.7Vpp into 75 Ohm load)
Green	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
Blue	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
GND	Ground
VGACLK0 VGADAT0	Digital serial I/O signals used for monitor detection (DDC1 specification)
HSYNC	Horizontal sync
VSYNC	Vertical sync

Note*: Although the VGA serial detection signals are supported on J8, a +5V power source is not provided. Additionally, the legacy "Monitor ID" signals are not provided.*

4.7 USB 2.0 (J10)

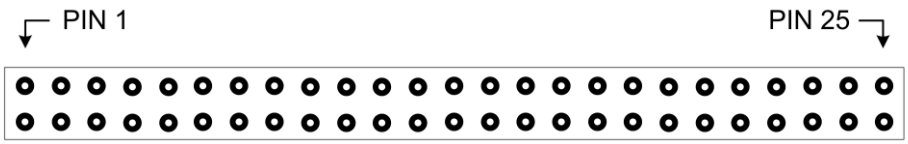
Connector J10 provides the data signals and power for USB ports 0–3. Each USB port supports 480 Mbps maximum transfer rates and is compliant with the USB 2.0 specification. This connector also mates with Neptune's optional Panel I/O Board, resulting in the USB ports being routed to standard PC-style connectors.

(not used)	**1**	**2**	Shield
GND	**3**	**4**	GND
USB3 data+	**5**	**6**	USB2 data+
USB3 data-	**7**	**8**	USB2 data-
USB3 power	**9**	**10**	USB2 power
(not used)	**11**	**12**	Shield
GND	**13**	**14**	GND
USB1 data+	**15**	**16**	USB0 data+
USB1 data-	**17**	**18**	USB0 data-
USB1 power	**19**	**20**	USB0 power

Signal	***Definition***
Shield	Ground for USB cable shield
USB0-3 power	Switched +5V for powering USB ports 0-3
USB0-3 data+	data + for USB ports 0-3
USB0-3 data-	data - for USB ports 0-3
GND	Ground

4.8 CompactFlash (J12)

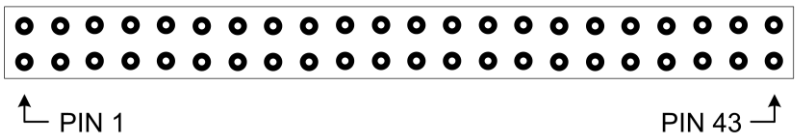
Connector J12 — located on the bottom side of the Neptune Baseboard — is a standard 50-pin CompactFlash socket. The socket connects to Neptune's primary IDE channel, and is configured such that the CF card is the system's primary Master IDE device.



GND1	**1**	**26**	(not used)
D3	**2**	**27**	D11
D4	**3**	**28**	D12
D5	**4**	**29**	D13
D6	**5**	**30**	D14
D7	**6**	**31**	D15
CE1	**7**	**32**	CE2
A10	**8**	**33**	(not used)
OE	**9**	**34**	IORD-
A9	**10**	**35**	IOWR-
A8	**11**	**36**	(not used)
A7	**12**	**37**	RDY
VCC	**13**	**38**	VCC
A6	**14**	**39**	CSEL
A5	**15**	**40**	(not used)
A4	**16**	**41**	RESET-
A3	**17**	**42**	WAIT
A2	**18**	**43**	INPACK
A1	**19**	**44**	REG
A0	**20**	**45**	ACT_SLV
D0	**21**	**46**	PDIAG
D1	**22**	**47**	D8
D2	**23**	**48**	D9
IOCS16	**24**	**49**	D10
GND25	**25**	**50**	CD2

4.9 IDE (J13, J14)

Standard IDE device interfaces are provided by two connectors — J13 (primary IDE) and J14 (primary IDE) — which have similar pinouts and signal assignments. Up to two devices can be connected to the primary IDE interface including a flashdisk, a hard disk or a CompactFlash disk on connector J12. Refer to the ETX CPU module's user manual for further details on the signals associated with these two connectors.



Reset-	**1**	**2**	GND
D7	**3**	**4**	D8
D6	**5**	**6**	D9
D5	**7**	**8**	D10
D4	**9**	**10**	D11
D3	**11**	**12**	D12
D2	**13**	**14**	D13
D1	**15**	**16**	D14
D0	**17**	**18**	D15
GND	**19**	**20**	Key
DRQ	**21**	**22**	GND
IDEIOW-	**23**	**24**	GND
IDEIOR-	**25**	**26**	GND
IORDY	**27**	**28**	GND
DACK-	**29**	**30**	GND
IRQ5	**31**	**32**	(not used)
A1	**33**	**34**	CBLID
A0	**35**	**36**	A2
CS1-	**37**	**38**	CS3-
LED-	**39**	**40**	GND
+5V	**41**	**42**	+5V
GND	**43**	**44**	(not used)

4.10 LCD LVDS Interface (J16)

Connector J16 provides access to LVDS LCD display interface signals that originate on the ETX CPU module that is attached to the Neptune baseboard.

Note: *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

GND	**1**	**2**	GND
LCD_D6	**3**	**4**	LCD_D16
LCD_D7	**5**	**6**	LCD_D17
GND	**7**	**8**	GND
LCD_D0	**9**	**10**	LCD_D10
LCD_D1	**11**	**12**	LCD_D11
GND	**13**	**14**	GND
LCD_D4	**15**	**16**	LCD_D12
LCD_D5	**17**	**18**	LCD_D13
GND	**19**	**20**	GND
LCD_D2	**21**	**22**	LCD_D14
LCD_D3	**23**	**24**	LCD_D15
GND	**25**	**26**	GND
VDD	**27**	**28**	VDD
VDD	**29**	**30**	VDD

Signal	***Definition***
LCD_D0-LCD_D17	LVDS-LCD data output (differential pairs)
VDD	Switched +3.3V power for use by display
GND	Ground

4.11 LCD LVDS Control (J17)

Connector J17 provides LCD-LVDS control signals. These are dependent on the functions provided by the attached ETX CPU module.

Note: *The signals on this connector's pins are defined by the ETX CPU module; refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

+12V	**1**	**2**	GND
GND	**3**	**4**	LCD_LTGIO0
LCD_BIASON	**5**	**6**	VGA_DET-
DISP_DIGON	**7**	**8**	JILI_DAT
LCD_BLON-	**9**	**10**	JILI_CLK

Signal	***Definition***
+12V	Switched +12V power for use by display
LCD_LTGIO0	General purpose I/O
LCD_BIASON	Flat panel contrast voltage control
LCD_BLON-	Flat panel backlight power control
VGA_DET-	Flat panel hot plug detection
DISP_DIGON	Flat panel digital power control
JILI_CLK	Flat panel parameter EEPROM I^2C clock
JILI_DAT	Flat panel parameter EEPROM I^2C data
GND	Ground

4.12 Audio (J18)

Audio connectivity is provided by connector J18. This connector also mates with Neptune's optional Panel I/O Board, resulting in the audio signals being routed to standard PC-style connectors.

Note: *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

SND_L	**1**	**2**	SND_R
ASGND	**3**	**4**	AUX_L
AUX_R	**5**	**6**	ASGND
MIC	**7**	**8**	ASVCC
(not used)	**9**	**10**	ASGND

Signal	***Definition***
SND_L/SND_R	Line-level output (left/right), capable of driving headphones, which is referred to as "Headphone Out" in most sound documentation
AUX_L/AUX_R	Line-Level input (left/right), which is referred to as "Line In" in most sound documentation
MIC	Microphone-level mono input; phantom power provided on pin 9
ASVCC	Microphone power reference
ASGND	Audio ground

4.13 Utility (J22)

Neptune's Utility connector provides signals for connection of an external speaker, "power good" input, and an ATX-style power button. This connector also mates with Neptune's optional Panel I/O Board, resulting in its signals being routed to functions on the I/O panel.

Speaker	1	2	+5V out
ATX power button	3	4	Key
GND	5	6	GND
Power good in	7	8	Key

Signal	*Definition*
Speaker	The digital signal on the Speaker pin is referenced to +5V out. Connect a speaker between this pin and +5V (available on pin 2)
+5V out	Switched +5V power output
ATX power button	Function varies; see discussion following this table
Power good in	Power good signal for use by on-board power management logic
GND	Ground

4.13.1 ATX Power Button Considerations

The ATX power button should be tied to ground whenever the "Power Button" is used. The "Power Button" has different functionality, depending on the current system mode and software operation. In general, the following guidelines apply:

- If the board is powered down, toggling (i.e., tie to ground briefly, then release) this button turns the system on, causing all non-standby voltages to become active.

  Note: *depending on the default configuration, the system usually powers-up immediately when power is applied to the system.*

- If the system is currently powered up and active, toggling (i.e., tie to ground briefly, then release) this button causes a system power-down event to be initiated. Typically, this powers-down the monitor, hard drive, and any other non-essential functions. The system must be operating and the software executing normally for this function. Under Windows and some other OSes, this power-down event may cause the system to shut down. Typically, this is software-configurable via an option setting for the given OS.
- If the system is currently powered-up and active, holding this button for four seconds causes a forced system shutdown. This is a hardware power-down, which can be detrimental to many OSes due to the fact that they are not given adequate time to initiate shut-down sequencing. This operation should only be used in critical circumstances, such as when the system itself is locked due to system instability or a software crash. After powering the system down in this manner, the system remains powered down until the power button is toggled (tied to ground again and released).

When ATX is enabled, a momentary contact between this pin and Ground causes the CPU to turn on and a contact of four seconds or longer generates a power shutdown.

4.14 HDD Power (J23)

The external hard drive power supply is provided by connector J23.

1	+5V out
2	GND
3	GND
4	+12V out

Signal	*Definition*
+5V out	Switched +5V for powering a hard drive or other peripheral
+12V out	Switched +12V for powering a hard drive or other peripheral
GND	Ground

4.15 ETX Ethernet (J24)

A 10/100 Ethernet connection is provided by connector J24. This connector also mates with Neptune's optional Panel I/O Board, resulting in the Ethernet interface being routed to a standard PC-style connector.

> ***Note:*** *The signals on this connector's pins are defined by the ETX CPU module. Please refer to the particular ETX module's user manual for further details on the definition and utilization of these signals.*

EGND	**1**	**2**	(not used)
TX+	**3**	**4**	TX-
RX+	**5**	**6**	LI_LED
(not used)	**7**	**8**	RX-
(not used)	**9**	**10**	ACT_LED

Signal	*Definition*
TX+/TX-	Ethernet transmit differential pair
RX+/RX-	Ethernet receive differential pair
EGND	Ethernet ground/shield
LI_LED	Link LED
ACT_LED	Activity LED

4.16 Analog I/O (J30)

Connector J30 provides the data acquisition subsystem's analog input and output signals. Pins 1-32 are the analog inputs, labeled as VINx for single-ended, and X+ or X- for differential.

VIN0 / 0+	**1**	**2**	VIN16 / 0-
VIN1 / 1+	**3**	**4**	VIN17 / 1-
VIN2 / 2+	**5**	**6**	VIN18 / 2-
VIN3 / 3+	**7**	**8**	VIN19 / 3-
VIN4 / 4+	**9**	**10**	VIN20 / 4-
VIN5 / 5+	**11**	**12**	VIN21 / 5-
VIN6 / 6+	**13**	**14**	VIN22 / 6-
VIN7 / 7+	**15**	**16**	VIN23 / 7-
VIN8 / 8+	**17**	**18**	VIN24 / 8-
VIN9 / 9+	**19**	**20**	VIN25 / 9-
VIN10 / 10+	**21**	**22**	VIN26 / 10-
VIN11 / 11+	**23**	**24**	VIN27 / 11-
VIN12 / 12+	**25**	**26**	VIN28 / 12-
VIN13 / 13+	**27**	**28**	VIN29 / 13-
VIN14 / 14+	**29**	**30**	VIN30 / 14-
VIN15 / 15+	**31**	**32**	VIN31 / 15-
GNDA	**33**	**34**	VOUT0
VOUT1	**35**	**36**	VOUT2
VOUT3	**37**	**38**	GNDA
(not used)	**39**	**40**	GND

Signal	***Definition***
VIN0-VIN31	16-bit analog input channels 0-31
VOUT0-VOUT3	12-bit analog output channels 0-3
GNDA	0V analog reference
GND	Ground

Note: *The reference grounds are NOT decoupled from the power grounds. They are indirectly connected to the power supply input (and other on-board ground/0V references). Do not assume that these grounds are floating, and do not apply a high-voltage input (relative to the power input ground) to these ground signals or to any other board I/O pin.*

4.17 Digital I/O (J31)

Connector J31 provides the data acquisition subsystem's programmable digital I/O signals. The signal functions are defined in the table that follows.

A0	**1**	**2**	A1
A2	**3**	**4**	A3
A4	**5**	**6**	A5
A6	**7**	**8**	A7
B0	**9**	**10**	B1
B2	**11**	**12**	B3
B4	**13**	**14**	B5
B6	**15**	**16**	B7
C0	**17**	**18**	C1
C2	**19**	**20**	C3
C4	**21**	**22**	C5
C6	**23**	**24**	C7
DIN0/CLK0	**25**	**26**	DIN1/GATE0
DOUT0/CTROUT0	**27**	**28**	DOUT2/CTROUT2
AD_RCB	**29**	**30**	DOUT1/SHOUT
DIN3/EXTCLK	**31**	**32**	DIN2/EXTGATE
+5V out	**33**	**34**	GND

Signal	*Definition*
A0-A7	Digital I/O port A; programmable direction
B0-B7	Digital I/O port B; programmable direction
C0-C7	Digital I/O port C; programmable direction
DIN0-DIN3	Digital input port with counter/timer and external trigger functions
DOUT0-DOUT2	Digital output port with counter/timer functions
CLK0	Input source to Counter 0
GATE0	Pin to control gating of Counter 0
CTROUT0	Counter 0 output
CTROUT1	Counter 1 output
AD_RCB	A/D convert signal output; can be used to synchronize multiple boards
SHOUT	Sample/hold output
EXTCLK	External A/D trigger input; Also used for digital interrupt (DINT) input
EXTGATE	Pin to control gating of counters 0 and 1 for A/D timing
+5V out	Switched +5V power output. ***Caution**: **Do not connect this pin to an external power supply!***
GND	Digital ground (0V - reference); used for digital circuitry only

4.18 Optoisolated I/O (J33)

Eight optoisolated input ports and eight optoisolated output ports are available on connector J33.

VCC0_OUT	**1**	**2**	OUT0_OUT
GND0_OUT	**3**	**4**	VCC1_OUT
OUT1_OUT	**5**	**6**	GND1_OUT
VCC2_OUT	**7**	**8**	OUT2_OUT
GND2_OUT	**9**	**10**	VCC3_OUT
OUT3_OUT	**11**	**12**	GND3_OUT
VCC4_OUT	**13**	**14**	OUT4_OUT
GND4_OUT	**15**	**16**	VCC5_OUT
OUT5_OUT	**17**	**18**	GND5_OUT
VCC6_OUT	**19**	**20**	OUT6_OUT
GND6_OUT	**21**	**22**	VCC7_OUT
OUT7_OUT	**23**	**24**	GND7_OUT
A0_IN	**25**	**26**	B0_IN
A1_IN	**27**	**28**	B1_IN
A2_IN	**29**	**30**	B2_IN
A3_IN	**31**	**32**	B3_IN
A4_IN	**33**	**34**	B4_IN
A5_IN	**35**	**36**	B5_IN
A6_IN	**37**	**38**	B6_IN
A7_IN	**39**	**40**	B7_IN

Signal	***Definition***
VCC0_OUT – VCC7_OUT	External voltage
GND0_OUT – GND7_OUT	Ground
OUT0_OUT – OUT7_OUT	Optoisolated outputs
A0_IN, B0_IN . . . A7_IN, B7_IN	External voltage input pairs, into FPGA

4.19 COM1-COM4 (J34)

Connector J34 provides access to Neptune's COM1-COM4 serial ports. COM1 and COM2 are associated with a controller located on the ETX CPU module, whereas the controller for COM3 and COM4 is located on the Neptune baseboard.

Each of these four ports is independently configurable in software for RS-232, RS-422, or RS-485 serial interface protocols. Additionally, each may be independently enabled or disabled.

Optional termination resistors for RS-422 and RS-485 operation are also selectable via jumper-group J45 (see Section 5 of this document).

Connector J34 mates with Neptune's optional Panel I/O Board, resulting in the COM1 and COM2 signals being routed to standard PC-style serial connectors.

Port No.	***Pin Assignment***
COM1	Pins 1–10
COM2	Pins 11–20
COM3	Pins 21–30
COM4	Pins 31–40

The following tables list the signals present on each J34 pin within these four groups of 10 pins. The signals in each group vary according to the selected serial interface protocol.

4.19.1 RS-232 Pin Assignment

COM1:	DCD1	**1**	**2**	DSR1
	RXD1	**3**	**4**	RTS1
	TXD1	**5**	**6**	CTS1
	DTR1	**7**	**8**	RI1
	GND	**9**	**10**	(Unused)
COM2:	DCD2	**11**	**12**	DSR2
	RXD2	**13**	**14**	RTS2
	TXD2	**15**	**16**	CTS2
	DTR2	**17**	**18**	RI2
	GND	**19**	**20**	(not used)
COM3:	DCD3	**21**	**22**	DSR3
	RXD3	**23**	**24**	RTS3
	TXD3	**25**	**26**	CTS3
	DTR3	**27**	**28**	RI3
	GND	**29**	**30**	(not used)
COM4:	DCD4	**31**	**32**	DSR4
	RXD4	**33**	**34**	RTS4
	TXD4	**35**	**36**	CTS4
	DTR4	**37**	**38**	RI4
	GND	**39**	**40**	(not used)

Signal	***Definition***	***DE-9 Pin***	***Direction***
DCD*n*	Data Carrier Detect	pin 1	Input
DSR*n*	Data Set Ready	pin 6	Input
RXD*n*	Receive Data	pin 2	Input
RTS*n*	Request to Send	pin 7	Output
TXD*n*	Transmit Data	pin 3	Output
CTS*n*	Clear to Send	pin 8	Input
DTR*n*	Data Terminal Ready	pin 4	Output
RI*n*	Ring Indicator	pin 9	Input
GND	Ground	--	--

4.19.2 RS-485 Pin Assignment

COM1:	NC	**1**	**2**	NC
	TXD/RXD+1	**3**	**4**	TXD/RXD-1
	GND	**5**	**6**	NC
	NC	**6**	**8**	NC
	GND	**7**	**10**	NC
COM2:	NC	**11**	**12**	NC
	TXD/RXD+2	**13**	**14**	TXD/RXD-2
	GND	**15**	**16**	NC
	NC	**17**	**18**	NC
	GND	**19**	**20**	NC
COM3:	NC	**21**	**22**	NC
	TXD/RXD+3	**23**	**24**	TXD/RXD-3
	GND	**25**	**26**	NC
	NC	**27**	**28**	NC
	GND	**29**	**30**	NC
COM4:	NC	**31**	**32**	NC
	TXD/RXD+4	**33**	**34**	TXD/RXD-4
	GND	**35**	**36**	NC
	NC	**37**	**38**	NC
	GND	**39**	**40**	NC

Signal	***Definition***	***DE-9 Pin***	***Direction***
TXD/RXD+*n*	Differential Transceiver Data (HIGH)	pin 2	bidirectional
TXD/RXD-*n*	Differential Transceiver Data (LOW)	pin 7	bidirectional
GND	Ground	--	--
NC	(not connected)	--	--

4.19.3 RS-422 Pin Assignment

COM1:	NC	**21**	**22**	NC
	TXD+1	**23**	**24**	TXD-1
	GND	**25**	**26**	RXD-1
	RXD+1	**27**	**28**	NC
	GND	**29**	**30**	NC
COM2:	NC	**31**	**32**	NC
	TXD+2	**33**	**34**	TXD-2
	GND	**35**	**36**	RXD-2
	RXD+2	**37**	**38**	NC
	GND	**39**	**40**	NC
COM3:	NC	**21**	**22**	NC
	TXD+3	**23**	**24**	TXD-3
	GND	**25**	**26**	RXD-3
	RXD+3	**27**	**28**	NC
	GND	**29**	**30**	NC
COM4:	NC	**31**	**32**	NC
	TXD+4	**33**	**34**	TXD-4
	GND	**35**	**36**	RXD-4
	RXD+4	**37**	**38**	NC
	GND	**39**	**40**	NC

Signal	***Definition***	***DE-9 Pin***	***Direction***
TXD+*n*/TXD-*n*	Differential transmit data	--	Output
RXD+*n*/RXD-*n*	Differential receive data	--	Input
GND	Ground	--	--
NC	(not connected)	--	--

4.20 COM5-COM6 (J37)

Connector J37 provides connectivity for serial I/O ports COM5 and COM6, which are associated with a controller on the Neptune Baseboard. RS-232 or TTL signal levels may be independently selected for these ports using jumper block J11. Unlike COM1-COM4, these two ports do not support RS-422 or RS-485 interface protocols.

DCD5	**1**	**2**	DSR5
RXD5	**3**	**4**	RTS5
TXD5	**5**	**6**	CTS5
DTR5	**7**	**8**	RI5
GND	**9**	**10**	(not used)
DCD6	**11**	**12**	DSR6
RXD6	**13**	**14**	RTS6
TXD6	**15**	**16**	CTS6
DTR6	**17**	**18**	RI6
GND	**19**	**20**	(not used)

Signal	***Definition***
DCD5/6	Port 5/6 Data Carrier Detect
RXD5/6	Port 5/6 Receive Data
TXD5/6	Port 5/6 Transmit Data
DTR5/6	Port 5/6 Data Terminal Ready
DSR5/6	Port 5/6 Data Set Ready
RTS5/6	Port 5/6 Request To Send
CTS5/6	Port 5/6 Clear To Send
RI5/6	Port 5/6 Ring Indicator
GND	Ground

4.21 Gigabit LED Connector (J39)

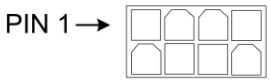
J39 provides signals for cabling to gigabit LAN status LEDs. The LED displays green when the connected LAN's speed is 1000 Mbps (gigabit), and orange or yellow when the speed is 100 Mbps.

Note: *These LEDs require a current-limiting resistor in the range of 220 to 270 ohms.*

Activity LED+	**1**	**2**	Activity LED-
Speed LED 1000-/100+	**3**	**4**	Speed LED 1000+/100-

4.22 ATX-style Input Power (J44)

Neptune can be connected to an external power supply via connector J44. Refer to the table below for a description of each pin's function.



PS_ON	**1**	**2**	+5V standby
GND	**3**	**4**	+5V in
GND	**5**	**6**	+5V in
+12V in	**7**	**8**	GND

Signal	***Definition***
+5V in	+5V DC input power. Range should be +4.75V to +5.25V measured at this connector. ***Note:*** *See discussion following this table.*
+12V in	Pass-through power for 12V-powered devices, including hard drives, auxiliary power, modules on the PC/104-*Plus* stack, and LCD backlight. Range should be +11.9V to +13.5V measured at this connector.
+5V standby	+5V standby power input. Powers board when in standby mode.
PS_ON	Power Supply ON. Feedback pin for external ATX supply, when needed; pulled low when on-board power is inactive.
GND	0-V (ground) power return path.

4.22.1 ATX-style Input Power Considerations

The Neptune baseboard and its attached ETX CPU module can be operated from a power supply voltage of +4.75 to +5.25 VDC supplied via its ATX-style power input connector (J44), with a few restrictions.

The "+12V in" power supply input provides a "pass through" power option for use with various peripherals and add-on modules. These include modules on the PC/104-*Plus* expansion stack, power for disk drives (through connector J2, described above), and LCD backlight power supplies. If these devices are not used, the "+12V in" input may be left unconnected.

Make certain that the power supply has sufficient current capacity to drive the system. The Neptune baseboard and attached ETX COM require 12 to 20 Watts or more, depending on the specific ETX COM being used and on the requirements of add-on modules and external peripherals that may require pass-through power. This could require over 4A on the "+V in" line at minimum voltage inputs. In particular, many disk drives need extra current during startup. If the system fails to boot properly or if disk accesses do not work correctly, the first thing to check is the power supply voltage level. Many boot-up problems result from insufficient voltage due to excess current draw on the "+Vin" supply during initialization.

Multiple +5V and ground pins are provided for extra current carrying capacity, if needed. Each pin is rated at 3A max (15W).

ATX control enables the +5V and +12V power to be switched on and off with an external momentary switch. A short press on the switch turns power on, and holding the switch on for four seconds or longer turns power off (see the description for connector J22, above).

4.23 Gigabit Ethernet (T1)

T1, an RJ-45 connector, provides Neptune's gigabit Ethernet interface, which is associated with an Intel 82541ER Ethernet controller located on the Neptune Baseboard.

RJ-45 Pin	*Signal*	*Definition*
1	BI_DA+	Bidirectional data pair +A
2	BI_DA-	Bidirectional data pair –A
3	BI_DB+	Bidirectional data pair +B
4	BI_DC+	Bidirectional data pair +C
5	BI_DC-	Bidirectional data pair –C
6	BI_DB-	Bidirectional data pair –B
7	BI_D+	Bidirectional data pair +D
8	BI_D-	Bidirectional data pair -D

4.24 SATA (SATA1, SATA2)

Connectors SATA1 and SATA2 are located on the top of the AMD ETX computer-on-module. Both connectors are industry standard SATA connectors and both have the same pin out as shown below.

1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

4.25 LPC (LPC1)

Connector LPC1 is located on the top of the AMD ETX computer-on-module. It is a Hirose FPC12-14P-P0.5 connector with the pin out as shown below.

LAD0	1	2	LAD1
LAD2	3	4	LAD3
GND	5	6	LFRAME#
INT_SERIRQ	7	8	BUF_PLT_RST#
GND	9	10	PCLK_CONN
GND	11	12	GND
+3.3V	13	14	+3.3V

4.26 DDI (DDI1)

Connector DDI1 is located on the top of the AMD ETX computer-on-module. It is a Hirose FH12-26S-0.5SH connector with the pin out as shown below.

GND	1	2	DDI_TX0+
DDI_TX0-	3	4	GND
DDI_TX1+	5	6	DDI_TX1-
GND	7	8	DDI_TX2+
DDI_TX2-	9	10	GND
DDI_TX3+	11	12	DDI_TX3-
GND	13	14	N/C
DDI_AUX+	15	16	DDI_AUX-
GND	17	18	DDI_HPD
SMB_DAT	19	20	SMB_CLK
GND	21	22	GND
GND	23	24	+3.3V
+3.3V	25	26	+5V

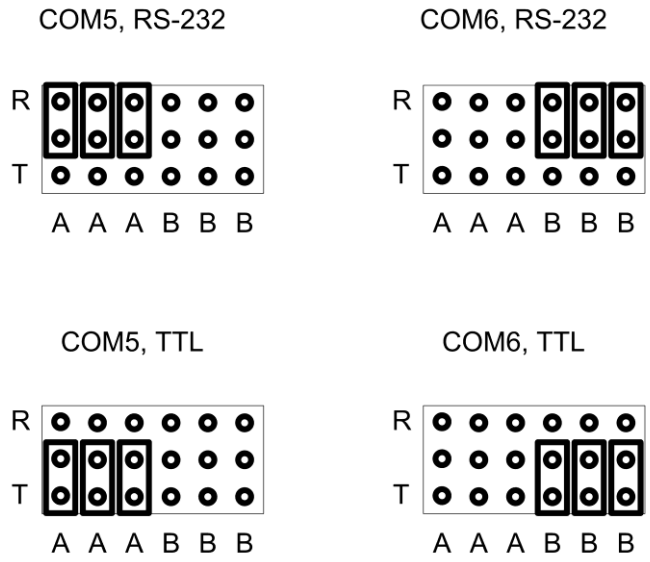
5. CONFIGURATION JUMPER DETAILS

This section describes the use of the Neptune Baseboard's configuration jumper options and indicates the default settings when appropriate.

5.1 Serial I/O TTL/RS-232 Selection (J11)

Jumper J11 is used for selecting either RS-232 or TTL levels for serial ports COM5 and COM6, connector J34.

Jumper block labels "AAA" applies to the COM5 port and labels "BBB" applies to the COM6 port. Using the common center row of pins, pins in the row labeled "R" are used to select RS-232 operation, and pins in the row labeled "T" are used to select TTL operation. All three jumpers must be inserted for a port, as shown in the example, below, for either RS-232 or TTL operation.



Default setting: *COM and COM6 jumpered for RS-232*

5.2 DMA/IRQ/Address/Bus Configuration (J26)

Jumper J26 is used to configure DMA level, IRQ level, base address and bus width.

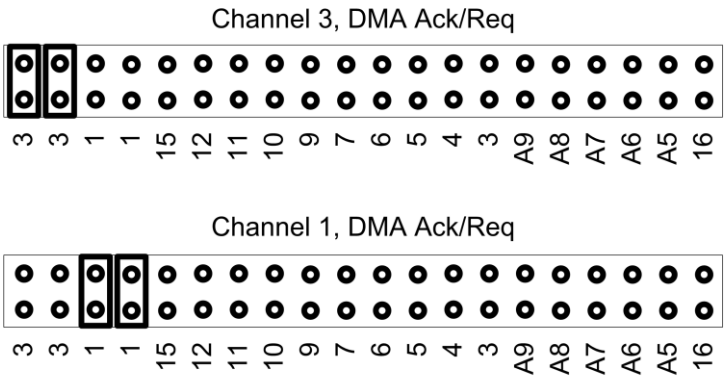
Pin Label	***Function***
3, 3 1, 1	DMA Level Configuration
15, 12, 11, 10, 9, 7, 6, 5, 4, 3	IRQ Level Configuration
A9, A8, A7, A6, A5	Base Address Selection
16	Bus Width Selection

The J26 jumper settings for each function are described on the next page.

5.2.1 DMA Level Configuration

Jumper J26 pins labeled 3, 3, 1, and 1 are used to configure DMA acknowledge and DMA request for DMA channels 1 and 3. Refer to the table and illustrations below.

Pin Label	*DMA Channel/Function*
3	Channel 3, DMA Acq
3	Channel 3, DMA Req
1	Channel 1, DMA Acq
1	Channel 1, DMA Req

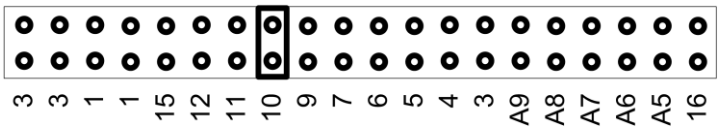


Default setting: *DMA Ack/Req for Channel 3 and Channel 1*

5.2.2 IRQ Level Configuration

Jumper J26 pins, labeled 15, 12, 11, 10, 9, 7, 6, 5, 4, and 3 are used for IRQ level configuration for data acquisition IRQ. Jumper the pin for the desired IRQ level; the pin label corresponds to the IRQ level.

The figure below shows an example of setting IRQ level 10.



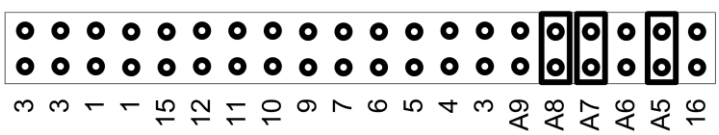
Default setting: *IRQ 10.*

5.2.3 Base Address Selection

Jumper J26 pins, A9, A8, A7, A6, and A5 are used to set the I/O registers base address. (Note: In = jumpered; Out = not jumpered.)

Base	*A9*	*A8*	*A7*	*A6*	*A5*
000h	In	In	In	In	In
020h	In	In	In	In	Out
040h	In	In	In	Out	In
060h	In	In	In	Out	Out
080h	In	In	Out	In	In
0A0h	In	In	Out	In	Out
0C0h	In	In	Out	Out	In
0E0h	In	In	Out	Out	Out
100h	In	Out	In	In	In
120h	In	Out	In	In	Out
140h	In	Out	In	Out	In
160h	In	Out	In	Out	Out
180h	In	Out	Out	In	In
1A0h	In	Out	Out	In	Out
1C0h	In	Out	Out	Out	In
1E0h	In	Out	Out	Out	Out
200h	Out	In	In	In	In
220h	Out	In	In	In	Out
240h	Out	In	In	Out	In
260h	Out	In	In	Out	Out
280h	Out	In	Out	In	In
2A0h	Out	In	Out	In	Out
2C0h	Out	In	Out	Out	In
2E0h	Out	In	Out	Out	Out
300h	Out	Out	In	In	In (default)
320h	Out	Out	In	In	Out
340h	Out	Out	In	Out	In
360h	Out	Out	In	Out	Out
380h	Out	Out	Out	In	In
3A0h	Out	Out	Out	In	Out
3C0h	Out	Out	Out	Out	In
3E0h	Out	Out	Out	Out	Out

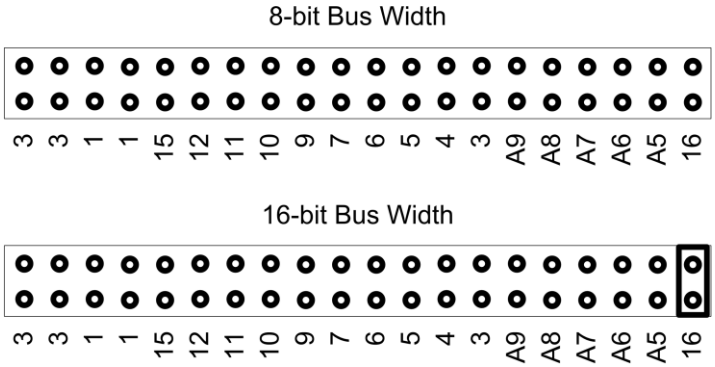
The figure below shows an example of setting a base address of 240h.



5.2.4 Bus Width Selection

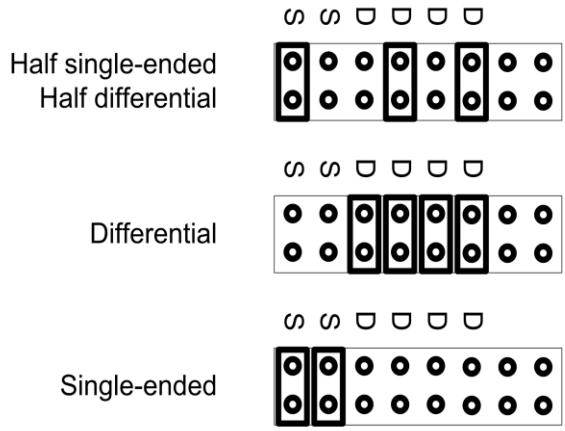
Use jumper J26, pin labeled 16, to select the desired bus width.

Bus Width	*Pin 16*
8-bit	Out
16-bit	In



5.3 Single-ended/Differential Selection (J28)

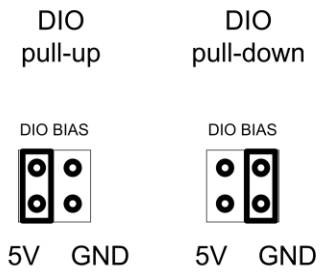
Use jumper J28, pins labeled D, S, to configure single-ended and differential operation, as shown in the figure below.



Default setting: *Single-ended*

5.4 DIO Pull-up/Pull-down Selection (J32)

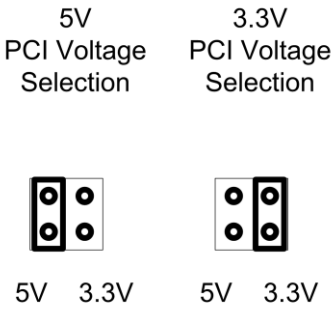
Jumper J32, as shown in the figure below, is used to configure DIO pull-up or pull-down.



Default setting: *DIO pull-down*

5.5 PCI Voltage Selection (J35)

Jumper J35, as shown in the figure below, is used to configure either +5V or +3.3V PCI voltage operation.



Default setting: *5V PCI Voltage Selection*

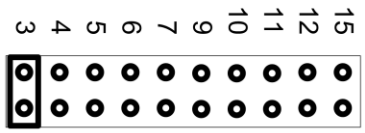
5.6 IRQ Selection (J38)

Use jumper J38 to select the desired interrupt request (IRQ) for serial ports COM3–COM6, as indicated in the table below. The jumper corresponding to the desired IRQ number *must* be installed for the interrupts to work on the serial ports.

For example, if all the ports are to be used at IRQ5, the jumper labeled IRQ5 must be installed.

Pin Label	***IRQ***
15	15
12	12
11	11
10	10
9	9
7	7
6	6
5	5
4	4
3	3

The figure below shows an example of selecting IRQ3.



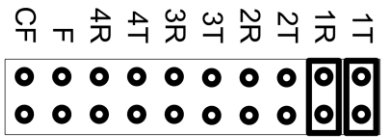
5.7 COM1-COM4 / CF Configuration (J40)

In RS-422 or RS-485 serial networks, termination resistors are normally installed at the endpoints of the cables to minimize reflections on the lines. The Neptune baseboard provides 150Ω resistors for this purpose. To enable resistor termination for a port, install jumpers in locations T and R of the configuration jumper block for the port, as shown below.

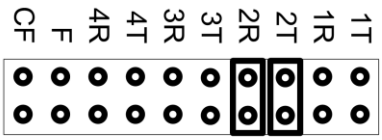
This jumper block also provides a jumper option for placing Neptune's shared printer/floppy interface in either printer or floppy mode, and a chip select for enabling/disabling the CompactFlash socket. Note, however, that the CompactFlash chip select jumper block is not used — that option is permanently shorted (via a zero ohm resistor) elsewhere on the circuit board.

Pin Label	*Function*
1T	COM1/Port 1 RS-422/RS-485 transmit
1R	COM1/Port 1 RS-422/RS-485 receive
2T	COM2/Port 2 RS-422/RS-485 transmit
2R	COM2/Port 2 RS-422/RS-485 receive
3T	COM3/Port 3 RS-422/RS-485 transmit
3R	COM3/Port 3 RS-422/RS-485 receive
4T	COM4/Port 4 RS-422/RS-485 transmit
4R	COM4/Port 4 RS-422/RS-485 receive
F	Not used
CF	CompactFlash chip select (not used; shorted elsewhere on the board)

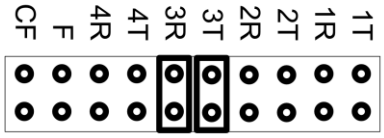
Port 1 Termination



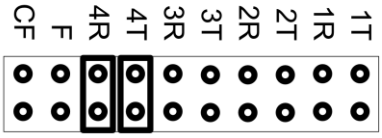
Port 2 Termination



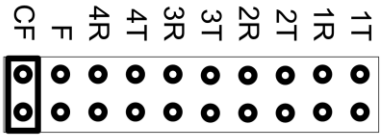
Port 3 Termination



Port 4Termination



Select CompactFlash



Default settings: *1T, 1R, 2T, 2R, 3T, 3R, 4T, 4R, F, and CF are installed.*

5.8 DAC Configuration (J43)

Use jumper J43 to configure the D/A converter for output voltage range, unipolar/bipolar mode, and clear.

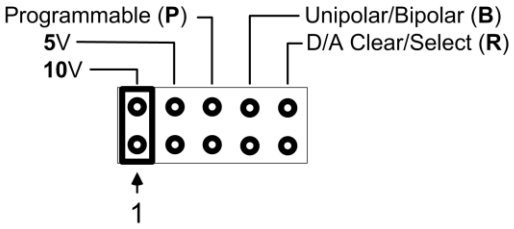
Pin Label	*DAC Configuration Function*
10	D/A range, ±10V
5	D/A range, ±5V
P	D/A range, programmable
B	Unipolar/bipolar
R	D/A clear select

Default settings: *"5" and "B" jumpers installed*

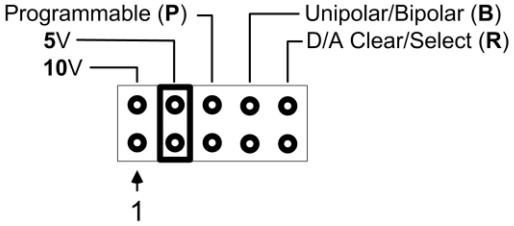
5.8.1 D/A Range

The illustrations below show the D/A range selection options for jumper J43.

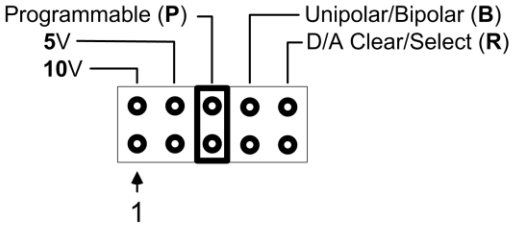
Range = ±10V



Range = ±5V



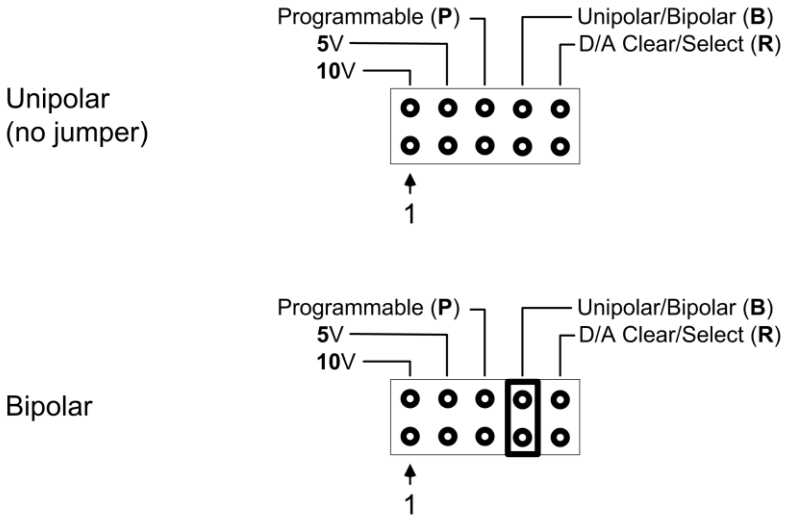
Range = programmable



Default setting: *+/-5V range jumper ("5") installed*

5.8.2 D/A Polarity

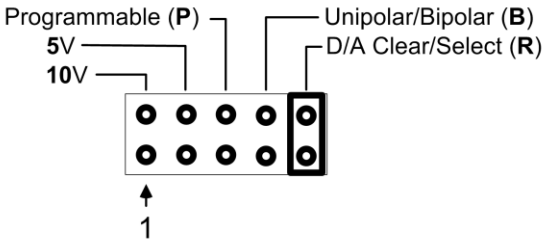
The illustrations below show the polarity selection options for J43.



Default setting: *Bipolar jumper ("B") installed*

5.8.3 D/A Clear Select

Jumper the "R" pin pair for clear select, as shown in the figure below.



Default setting: *D/A Clear/Select jumper ("R") not present*

6. NEPTUNE BASEBOARD I/O REGISTER MAP

6.1 Overview

The Neptune baseboard occupies 24 bytes in the system I/O address space. Registers 12 through 15 provide paged windows for access to additional registers without requiring additional I/O address space.

The following table summarizes the register functions and base address offsets for each page. Detailed bit-by-bit descriptions for each function follow thereafter.

Note: *Control bits in register 8 are used for page selection.*

Base +	***Write Function***	***Read Function***
0	Start A/D Conversion	A/D LSB (bits 7-0)
1	Auxiliary Digital Output	A/D MSB (bits 15-8)
2	A/D Low Channel Register	A/D Low Channel Read-Back
3	A/D High Channel Register	A/D High Channel Read-Back
4	D/A LSB Register	Auxiliary Digital Input
5	D/A MSB + Channel Register	
6	FIFO Depth Register	FIFO Depth Register
7	FIFO Control Register	FIFO Status Register
8	Miscellaneous Control Register	Status Register
9	Operation Control Register	Operation Status Register
10	Counter/Timer Control Register	Counter/Timer Control Read-back
11	Analog Configuration Register	Analog Configuration Read-back
12	(See paged registers, below)	
13	(See paged registers, below)	
14	(See paged registers, below)	
15	(See paged registers, below)	
16	Address Pointer/Enable Register	Address Pointer/Enable Register
17	Data for Address/IRQ No.	Read-Back of Address Registers
18	--	Interrupt Status Register
19	Optoisolated Output Data (Write)	Optoisolated Input Data (Read)
20	EEPROM Read/Write + Address	EEPROM Busy Status
21	EEPROM Data (Write)	EEPROM Data (Read)
22	Reload Command	N/A
23	N/A	N/A

Page 0 — 82C54 Counter/Timer Access		
Base +	**Write Function**	**Read Function**
12	Counter 0 Data	Counter 0 Data Read-back
13	Counter 1 Data	Counter 1 Data Read-back
14	Counter 2 Data	Counter 2 Data Read-back
15	82C54 Control	82C54 Control Read-back

Page 1 — 82C55-Type Digital I/O		
Base +	**Write Function**	**Read Function**
12	Port A Output	Port A Input
13	Port B Output	Port B Input
14	Port C Output	Port C Input
15	DIO Control Register	DIO Control Register Read-back

Page 2 — FIFO Control (Enhanced Feature Page)		
Base +	**Write Function**	**Read Function**
12	Expanded FIFO Threshold Register	Expanded FIFO Depth Read-back
13	N/A	N/A
14	N/A	N/A
15	N/A	N/A

Page 3 — Autocalibration Registers		
Base +	**Write Function**	**Read Function**
12	EEPROM/TrimDAC Data Latch	EEPROM/TrimDAC Data Read-back
13	EEPROM/TrimDAC Address Latch	EEPROM/TrimDAC Address Read-
14	EEPROM/TrimDAC Control Register	EEPROM/TrimDAC Status Register
15	Special Features Unlock Register	FPGA Revision Code

Page 4 — Not used		
Base +	**Write Function**	**Read Function**
12	This page is not available	
13		
14		
15		

Page 5 — D/A Waveform Generator (Enhanced Feature Page)		
Base +	**Write Function**	**Read Function**
12	Waveform Address Latch (LSB)	Waveform Address Latch (LSB)
13	Waveform Address Latch (MSB)	Waveform Address Latch (MSB)
14	Waveform Configuration Register	Waveform Configuration Read-Back
15	Waveform Command Register	

Page 6 — CPLD I/O Window (Enhanced Feature Page)		
Base +	**Write Function**	**Read Function**
12	Page 6 is a window to the CPLD I/O. This page should not be accessed in normal operation. Refer to the CPLD Specification for details.	
13		
14		
15		

6.2 Neptune Baseboard I/O Register Summary

6.2.1 Write Register Definitions

Base +	7	6	5	4	3	2	1	0
Main Register Set								
0	--Start A/D Conversion--							
1	-	-	-	-	LED	DOUT2	DOUT1	DOUT0
2	-	-	-	L4	L3	L2	L1	L0
3	-	-	-	H4	H3	H2	H1	H0
4	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
5	DACH1	DACH0	DASIM	DAGEN	DA11	DA10	DA9	DA8
6	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1
7	-	-	-	-	FIFOEN	SCANEN	FIFORST	-
8	-	-	RESETA	RESETD	INTRST	P2	P1	P0
9	ADINTE	DINTE	TINTE	RSVD1	DMAEN	-	CLKEN	CLKSEL
10	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN
11	-	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0
(See paged registers, below)								
16	ENABLE	-	-	-	-	A2	A1	A0
17	-	D6	D5	D4	D3	D2	D1	D0
18	-	-	-	-	-	-	-	-
19	OPTO_OUT7	OPTO_OUT6	OPTO_OUT5	OPTO_OUT4	OPTO_OUT3	OPTO_OUT2	OPTO_OUT1	OPTO_OUT0
20	R/W	EEA6	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
21	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
22	RELOAD	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	-
Page 0 — 82C54 Counter/Timer Access								
12	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0
13	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0
14	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0
15	SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Page 1 — 82C55-Type Digital I/O								
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14	C7	C6	C5	C4	C3	C2	C1	C0
15	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL
Page 2 — FIFO Control (Enhanced Feature Page)								
12	-	-	-	-	-	-	-	FT9
13	-	-	-	-	-	-	-	-
14	-	-	-	-	-	-	-	-
15	-	-	-	-	-	-	-	-
Page 3 — Autocalibration Registers								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	-	A6	A5	A4	A3	A2	A1	A0

Base +	7	6	5	4	3	2	1	0
14	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN	-	-	-
15	--FPGA Feature Unlock Register--							
Page 5 — D/A Waveform Generator (Enhanced Feature Page)								
12	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
13	-	-	-	-	-	-	DACA9	DACA8
14	DEPTH3	DEPTH2	DEPTH1	DEPTH0	WGCH1	WGCH0	WGSRC1	WGSRC0
15	-	-	-	-	WGINC	WGRST	WGPS	WGSTRT
Page 6 — CPLD I/O Window (Enhanced Feature Page)								
12	This page is a window to the CPLD I/O. Refer to the CPLD specification for details.							
13								
14								
15								

Note: *Page 4, Enhanced Feature Page, is not supported on Neptune.*

6.2.2 Read Register Definitions

Base +	7	6	5	4	3	2	1	0
Main Register Set								
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	-	-	-	L4	L3	L2	L1	L0
3	-	-	-	H4	H3	H2	H1	H0
4	DACBUSY	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0
5	-	-	-	-	-	-	-	FD9
6	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1
7	EF	HF	FF	OVF	FIFOEN	SCANEN	PAGE1	PAGE0
8	STS	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
9	ADINT	DINT	TINT	-	DMAEN	P2	CLKEN	CLKSEL
10	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN
11	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0
(See paged registers, below)								
16	ENABLE	-	-	-	-	A2	A1	A0
17		D6	D5	D4	D3	D2	D1	D0
18					INT3	INT2	INT1	INT0
19	OPTO IN7	OPTO IN6	OPTO IN5	OPTO IN4	OPTO IN3	OPTO IN2	OPTO IN1	OPTO IN0
20	BUSY	-	-	-	-	-	-	-
21	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
22	-	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	-
Page 0 — 82C54 Counter/Timer Access								
12	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0
13	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0
14	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0

Base +	7	6	5	4	3	2	1	0
15	SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Page 1 — 82C55-Type Digital I/O								
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14	C7	C6	C5	C4	C3	C2	C1	C0
15	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL
Page 2 — FIFO Control (Enhanced Feature Page)								
12	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-
14	-	-	-	-	-	-	-	-
15	-	-	-	-	-	-	-	-
Page 3 — Autocalibration Registers								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	-	A6	A5	A4	A3	A2	A1	A0
14	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0
15	--FPGA Revision Code--							
Page 5 — D/A Waveform Generator (Enhanced Feature Page)								
12	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
13	-	-	-	-	-	-	DACA9	DACA8
14	DEPTH3	DEPTH2	DEPTH1	DEPTH0	WGCH1	WGCH0	WGSRC1	WGSRC0
15	-	-	-	-	-	-	-	-
Page 6 — CPLD I/O Window (Enhanced Feature Page)								
12	This page is a window to the CPLD I/O. Refer to the CPLD specification for details.							
13								
14								
15								

Note: *Page 4, Enhanced Feature Page, is not supported on Neptune.*

6.3 Neptune Baseboard I/O Register Description

Note: *In the register descriptions below, writes to undefined bits have no effect. Reads of undefined bits return zeroes.*

Registers 0–11

Base+0 (Write) **Start A/D Conversion**

Bit:	7	6	5	4	3	2	1	0
Name:	ADSTART							

ADSTART Writing any value to this register starts an A/D conversion, unless a conversion is already in progress (AD_BUSY high). An A/D conversion starts even if the board is set up for interrupt, DMA, or external trigger mode.

Base+0 (Read) **A/D LSB (bits 7-0):**

Bit:	7	6	5	4	3	2	1	0
Name:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

If the FIFO is not empty, this register returns the LSB of the A/D value stored at the current FIFO pointer. If the FIFO is empty, reading from this register returns 0.

AD7-AD0 A/D data bits 7 - 0; AD0 is the LSB.

Base+1 (Write) **Auxiliary Digital Output:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	LED	DOUT2	DOUT1	DOUT0

LED Toggles the on-board user LED; 1 = on, 0 = off.

DOUT2-0 Auxiliary digital output bits on analog I/O header J31. Two pins also serve as optional counter outputs based on control register bits at Base+10:

DOUT2–J31, pin 28. Counter 2 output when OUT2EN = 1 (Base+10, bit 5).

DOUT1–J31, pin 30.

DOUT0–J31, pin 27. Counter 0 output when OUT0EN = 1 (Base+10, bit 4).

Base+1 (Read) **A/D MSB (bits 15-8):**

Bit:	7	6	5	4	3	2	1	0
Name:	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

If the FIFO is not empty, this register returns the MSB of the A/D value stored at the current FIFO pointer and decrements the FIFO depth value by 1 sample. If the FIFO is empty, reading from this register returns 0.

AD15–8 A/D data bits 15 - 8; AD15 is the MSB.

Base+2 (Read/Write) **A/D Low Channel:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	L4	L3	L2	L1	L0

L4–L0 The low channel number setting in the A/D channel scan range. Channel numbers range from 0 to 31 in single-ended mode. Writing to this register updates the current channel internal register.

Base+3 (Read/Write) **A/D high Channel**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	H4	H3	H2	H1	H0

H4–H0 The high channel number setting in the A/D channel scan range. Channel numbers range from 0 to 31 in single-ended mode.

Base+4 (Write) **DAC LSB**

Bit:	7	6	5	4	3	2	1	0
Name:	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7–DA0 D/A data bits 7 - 0 for the channel currently being accessed. This register is a holding register. Writing to it does not affect any D/A channel until the MSB is written. When the MSB is written (see below, Base+5), the value written to that register, along with the value written to this register, are simultaneously written to the D/A chip's load register for the selected channel. See Base+5, write for more details.

Base+4 (Read) **Status/Auxiliary Digital Input**

Bit:	7	6	5	4	3	2	1	0
Name:	DACBUSY	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0

DACBUSY 1 = Busy - The D/A serial transfer is in progress.
0 = Idle
Do not attempt to write to the D/A converters at Base+4 or Base+5 while this bit is high. This bit must be checked before any write to these registers. Any attempts to write to the D/A channels while this bit is high will be ignored.

CALBUSY 1 = Busy
0 = Idle
When CALBUSY = 1, calibration is in progress or EEPROM is being accessed. Do not attempt calibration or EEPROM access while this bit is high. This bit must be checked before any calibration or EEPROM operation is attempted.

ACACT This is a copy of the value found at Page 4, Base+14, bit 1. It is mirrored at this location to provide a page-independent means of seeing the AC status, since AC uses Page 3.

DIN3-DIN0 Auxiliary digital inputs on analog I/O header J31. These pins have multiple functions based on control bits at Base+9 and Base+10:
DIN3–J31, pin 31. External A/D clock when CLKSEL = 1 (Base+9 bit 0)
DIN2–J31, pin 32. Gate for counters 1 and 2 when GT12EN = 1 (Base+10 bit 0)
DIN1–J31, pin 26. Gate for counter 0 when GT0EN = 1 (Base+10 bit 2)
DIN0–J31, pin 25. Clock for counter 0 when SRC0 = 1 (Base+10 bit 1)

Base+5 (Write) **DAC MSB + Channel**

Bit:	7	6	5	4	3	2	1	0
Name:	DACH		DASIM	DAGEN	DA11	DA10	DA9	DA8

When this register is written, the D/A channel selected by DACH will be loaded using the currently stored D/A value in the registers. This is applicable when DASIM is 0.

DACH Binary number of the D/A channel, 0 — 3.

DASIM D/A simultaneous update.

NOTE: If enhanced features are disabled this is always '0' for backwards compatibility, meaning that D/A outputs will update on every write to this register.

1 = Latches D/A channel and output. Output will not change until this register is written to again with DASIM set to 0.

0 = Perform D/A simultaneous update. All previously latched D/A channels and current channel will update.

DAGEN D/A waveform generator enable

NOTE: If enhanced features are disabled this is always '0'.

1 = Data is transferred to the D/A wave form memory block instead of the DAC chip. Used in conjunction with D/A wave form generator to store DAC code.

0 = Data is transferred to the DAC chip for output.

DA11-8 D/A bits 11 – 8 for the selected output channel; DA11 is the MSB

Base+5 (Read) **FIFO Depth Read-back (bit 8):**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	FD9

This register provides the current FIFO depth in the enhanced mode. In the normal mode, this register is not used.

FD9 FIFO depth (bit 9). (See FIFO Threshold: Base+6, below)

Base+6 (Write) **FIFO Threshold:**

Bit:	7	6	5	4	3	2	1	0
Name:	FT8	FT7	FT6	FT5	FT4	FT3	FT2	FT1

FT8-FT1 FIFO threshold (bits 1-8). This is the level at which the board will generate an interrupt request when the FIFO is enabled (FIFOEN = 1 in Base+7). Note that the value written is shifted by 1 bit, i.e. divided by 2. For example, if you want a FIFO threshold of 256 samples, write a 128 to this register.

The interrupt routine must read exactly this number of samples out each time it runs. The last time the routine runs, it should read whatever is remaining in the FIFO by monitoring the EF bit (Empty Flag) in the FIFO status register at Base+7. When the FIFO is empty, EF = 1, and the FIFO returns the value hex FF on all read operations.

If you are sampling at a slow rate or want to control when the interrupt occurs, you can set the threshold to a low value. For example, if you are sampling 16 channels at 10 Hz and you want an interrupt each set of samples, you can set the threshold to 16 (write an 8 to this register), so that an interrupt will occur each 16 samples. Then the interrupt routine should read out 16 samples from the FIFO, and you get new data as soon as it is available.

For higher sample rates (100 KHz or higher) it may be necessary to increase the threshold above 256, to around 350 or even 512 with enhanced features enabled. If you set the threshold too high, you may overrun the FIFO, since the interrupt routine may not respond before the remaining locations are filled, causing an overflow. An overflow can be detected by checking the OVF bit in the FIFO status register at Base+7. The correct threshold for your application can only be determined by testing.

Base+6 (Read) **FIFO Depth:**

Bit:	7	6	5	4	3	2	1	0
Name:	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1

This register provides the current FIFO depth corresponding to the number of samples in the FIFO.

FD8-FD1 The current FIFO depth. It must be noted that the FIFO depth is the actual depth and not a number shifted as in case of the FIFO threshold.

Base+7 (Write) **FIFO Control**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	FIFOEN	SCANEN	FIFORST	-

FIFOEN FIFO enable:

1 = Enable FIFO operation; if interrupts are enabled, interrupts will occur when the FIFO hits threshold (TF = 1). This slows down the interrupt rate dramatically compared to the actual A/D sample rate.

0 = Disable FIFO operation; if interrupts are enabled, interrupts will occur after each A/D conversion.

SCANEN Scan enable:

1 = Scan mode enabled; FIFO will fill up with data for a single scan, and STS will stay high until entire scan is complete; if interrupts are enabled, interrupts will occur on integral multiples of scans.

0 = Scan mode disabled; The STS bit will correspond directly to the status indicator from the A/D converter.

FIFORST FIFO reset:

1 = Reset FIFO; after this command is issued, EF = 1, TF = 0, FF = 0 (in Base+7).

0 = No function.

Base+7 (Read) **FIFO Status:**

Bit:	7	6	5	4	3	2	1	0
Name:	EF	TF	FF	OVF	FIFOEN	SCANEN	PAGE	

EF Empty flag:

1 = FIFO is empty.

0 = FIFO is not empty.

TF Threshold flag:

1 = FIFO is at or beyond threshold; if the FIFO threshold is 256 words, this flag is set when the FIFO contains at least 256 words of A/D data.

0 = FIFO is less than threshold.

FF Full flag:

1 = FIFO is full; the next A/D conversion will result in an overflow.

0 = FIFO is less than full.

OVF Overflow flag:

1 = FIFO has overflowed; data has been lost. This flag is cleared on the next successful A/D read.

0 = FIFO has not overflowed since the last A/D data read.

FIFOEN FIFO enable read-back.

SCANEN Scan enable read-back.

PAGE Read-back of the current page register setting. See register Base+8 below.

Base+8 (Write) **Miscellaneous and Page Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	RESETA	RESETD	INTRST	PAGE		

RESETA Writing a 1 to this bit causes a full reset of all features of the board, including the DACs, the FIFO, the digital I/O, and all internal registers. The counter/timers are not affected by this reset.

RESETD Writing a 1 to this bit causes a reset identical to above except the analog outputs are not affected.

INTRST Writing a 1 to this bit resets the interrupt request circuit on the board. The programmer must write a 1 to this bit during the interrupt service routine, or further interrupts will not occur. Writing a 1 to this bit does not disturb the values of the PAGE bits.

PAGE Three-bit value that selects which I/O device is accessible through the registers at locations Base+12 through Base+15:

Bits <2:0>	***Page***	***Device***
000	0	8254
001	1	8255
010	2	FIFO Control
011	3	EEPROM/TrimDAC
100	4	Not Used
101	5	D/A Waveform
110	6	Factory Use Only
111	7	Not Used

Grayed pages (2, 4, 5, 6, and 7) are only accessible when the enhanced features are enabled. Notice that bit 2 is an enhanced feature bit.

Writing to the page bits will not generate a board reset or interrupt reset, as long as those bits are kept at 0 in the data written to this register.

Base+8 (Read) **A/D Status:**

Bit:	7	6	5	4	3	2	1	0
Name:	STS	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0

STS A/D chip status:
1 = A/D conversion or A/D scan in progress.
0 = A/D idle.

S/D1-0 Single-ended / Differential A/D input mode indicator. S/D1 controls the channels 8-15 and 24-31, S/D0 controls 0-7 and 16-23.
1 = Single-ended (default).
0 = Differential.

ADCH4-0 Current A/D channel; this is the channel currently selected on board and is the channel that will be used for the next A/D conversion (unless a new value is written to the low channel register).

Base+9 (Write) **Interrupt and A/D Clock Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	ADINTE	DINTE	TINTE	RSVD1	DMAEN	-	CLKEN	CLKSEL

ADINTE A/D interrupt enable:
1 = Enable A/D interrupt operation.
0 = Disable A/D interrupt operation.

DINTE Digital interrupt enable:
1 = Enable digital I/O interrupt operation.
0 = Disable digital I/O interrupt operation.

TINTE Timer 0 interrupt enable:
1 = Enable counter/timer 0 interrupt operation.
0 = Disable counter/timer 0 interrupt operation.

RSVD1 Reserved for future use

DMAEN DMA Enable. This bit is ignored if enhanced features are disabled. See DMA signal definition for more detail on DMA behavior.
1 = DMA Enabled.
0 = DMA Disabled.

CLKEN Enable hardware clock for A/D sampling:
1 = Enable hardware clock for A/D (source is selected with CLKSEL bit below);
NOTE: When this bit is 1, software triggers are disabled, i.e. writing to Base+0 will not start an A/D conversion.
0 = Disable hardware clocking for A/D; A/D conversions occur with software command only.

CLKSEL Hardware clock select (enabled only when CLKEN = 1 above):
1 = Internal clock: Falling edges on the output of counter/timer 2 generate A/D conversions. Counter 2 is in turn driven by counter 1, which is driven by the clock selected by bit FREQ12 in Base+10 below.
0 = External trigger: Falling edges on the DIN3/EXTCLK pin on the I/O header generate A/D conversions.

Base+9 (Read) **Interrupt and A/D Clock Status:**

Bit:	7	6	5	4	3	2	1	0
Name:	ADINT	DINT	TINT	-	DMAEN	P2	CLKEN	CLKSEL

ADINT A/D interrupt status; Cleared by writing to INTRST (Base+8).
1 = A/D interrupt request has occurred.
0 = No interrupt request.

DINT Digital interrupt status; Cleared by writing to INTRST (Base+8).
1 = Digital interrupt request has occurred.
0 = No interrupt request.

TINT Timer interrupt status; Cleared by writing to INTRST (Base+8).
1 = Timer interrupt request has occurred.
0 = No interrupt request.

DMAEN Read-back of control register bit defined, above.

P2 Read-back of P2 register bit defined at Base+8/write.

CLKEN Read-back of control register bit defined, above.

CLKSEL Read-back of control register bit defined, above.

Base+10 (Read/Write) **Counter/Timer and DIO Control**

Bit:	7	6	5	4	3	2	1	0
Name:	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN

FREQ12 Input frequency select for the counter 1-2 cascade:
1 = Input to counter 1 is a 100 KHz (one hundred, not ten) frequency derived from the on-board 10 MHz oscillator.
0 = Input to counter 1 is 10 MHz from the on-board oscillator.

FREQ0 Input frequency select for counter 0 when SRC0 = 1 (bit 1):
1 = Input to counter 0 is a 10 KHz (ten, not one hundred) frequency derived from the on-board 10 MHz oscillator.
0 = Input to counter 0 is 10 MHz from the on-board oscillator.

OUT2EN Counter/timer 2 output enable:
1 = Counter 2 output appears on I/O header J31, pin 28.
0 = J31, pin 28, is controlled by bit DOUT0 at Base+1.

OUT0EN Counter/timer 0 output enable:
1 = Counter 0 output appears on I/O header J31 pin 27, OUT 0 / DOUT 0.
0 =.OUT 0 / DOUT 0 pin is set by bit DOUT0 at Base+1.

RSVD Reserved for future use

GT0EN Counter/timer 0 gate enable:
1 = Gate 0 / DIN 1, J31 pin 26, acts as an active high gate for counter/timer 0. This pin is connected to a 10KΩ pull-up resistor.
0 = Counter/timer 0 runs freely with no gating.

SRC0 Counter 0 input source:
1 = Input to Counter 0 is the clock determined by FREQ0 (bit 6).
0 = Input to Counter 0 is J31 pin 25 (CLK 0 / DIN 0). The falling edge is active. This pin is connected to a 10KΩ pull-up resistor.

GT12EN Counter/timer 1/2 and external trigger gate enable:
This bit enables gating for A/D sampling for both internal and external clocking.
1 = When J31 pin 32 (EXTGATE / DIN 2) is low prior to the start of A/D conversions, A/D conversions will not begin until it is brought high (trigger mode).
If the pin is brought low while conversions are occurring, conversions will pause until it is brought high (gate mode). J31 pin 32 is connected to a 10KΩ pull-up resistor.
0 = The interrupt operation begins immediately once it is set up and the selected clock source begins, with no external triggering or gating.

Base+11 (Write) **Analog Configuration:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0

SCINT1-0 Scan interval. This is the time between A/D samples when performing a scan (SCANEN = 1). The driver sets a default of 10µs.

SCINT1	***SCINT0***	***Interval***
0	0	20µS
0	1	15µS
1	0	10µS
1	1	4µS

RANGE 5V or 10V A/D positive full-scale voltage (0 = 5V, 1 = 10V)

ADBU A/D bipolar/unipolar setting; 0 = bipolar, 1 = unipolar. These control bits define the A/D input range for a gain setting of 1.

RANGE	***ADBU***	***A/D Range***
0	0	+/- 5V
0	1	0-5V
1	0	+/- 10V
1	1	0-10V

G1-0 A/D programmable gain amplifier setting:

G1	***G0***	***Gain***
0	0	1
0	1	2
1	0	4
1	1	8

The gain setting is the ratio between the full-scale voltage range at the A/D converter and the full-scale voltage range at the input to the board. The gain should never cause the input signal to exceed the range of the A/D, because incorrect measurements will result (clipping).

The A/D full-scale voltage range is defined by the RANGE and ADBU bits above. To calculate the optimum gain setting, select the highest gain that does not allow the input signal to exceed the selected A/D range over its entire expected fluctuation range. Note that these settings can be changed at any time, even between A/D conversions, so you can tune the board's settings to each input signal.

Note: *On power-up or system reset, the board is configured for A/D bipolar mode, input range = ±5V, and gain = 1, corresponding to all zeros in this register.*

Base+11 (Read) **Analog I/O Read-back:**

Bit:	7	6	5	4	3	2	1	0
Name:	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0

WAIT Analog input circuit settling time hold-off indicator:
1 = The analog input circuit is settling on a new signal and is not yet ready for a new conversion to start; this will occur each time you change the channel, gain, or input range on the board. The wait time is approximately 10µs.
0 = The analog input circuit has settled and a new A/D conversion may begin.

RSVD Reserved for future use.

SCINT1-0 Read-back of control bit described, above. Only available if enhanced features are enabled.

RANGE Read-back of control bit described, above.

ADBU Read-back of control bit described, above.

G1-0 Read-back of control bit described, above.

6.3.1 Page 0 Register Definitions

This section is included as a reference to the FPGA's page 0 counter/timer registers. Behavior of these registers should be identical to the 82C54 counter/timer chip. Please read the 82C54 datasheet for this behavior.

Base+12 (Read/Write) **Counter 0 Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0

CRT0D7-0 Counter 0 data.

Base+13 (Read/Write) **Counter 1 Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0

CRT1D7-0 Counter 1 data.

Base+14 (Read/Write) **Counter 2 Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0

CRT2D7-0 Counter 2 data.

Base+15 (Read/Write) **82C54 Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1-0 Counter select.
RW1-0 Read/write mode.
M2-0 Timer mode.
BCD Binary Coded Decimal counter.

Note: *For more information refer the 82C54 datasheet.*

6.3.2 Page 1 Register Definitions

This section is included as a reference to the FPGA's page 1 82C55-like digital I/O registers. Behavior of these registers should be identical to the 82C55 counter/timer chip. Please read the 82C55 datasheet for this behavior.

Base+12 (Read/Write) **DIO Port A I/O:**

Bit:	7	6	5	4	3	2	1	0
Name:	A7	A6	A5	A4	A3	A2	A1	A0

This register is used for digital I/O on Port A. The direction of Port A is controlled by the DIO control register at Base+15 with the DIRA bit. When the port is configured as an output port, the output pins DIO A7–0 on connector J31 will be set to the values in this register. When the port is in input mode, the register will read back logic levels on pins DIO A7–0.

A7–A0 Port A data.

Base+13 (Read/Write) **DIO Port B I/O:**

Bit:	7	6	5	4	3	2	1	0
Name:	B7	B6	B5	B4	B3	B2	B1	B0

This register is used for digital I/O on Port B. The direction of Port B is controlled by the DIO control register at Base+15 with the DIRB bit. When the port is configured as an output port, the output pins DIO B7-0 on connector J31 will be set to the values in this register. When the port is in input mode, the register will read back logic levels on pins DIO B7–0.

B7-B0 Port B data.

Base+14 (Read/Write) **DIO Port C I/O:**

Bit:	7	6	5	4	3	2	1	0
Name:	C7	C6	C5	C4	C3	C2	C1	C0

This register is used for digital I/O on Port C. The direction of Port C is controlled by the DIO control register at Base+15 with the DIRCH and DIRCL bits. When the port is configured as an output port, the output pins DIO C7-0 on connector J31 will be set to the values in this register. When the port is in input mode, the register will read back logic levels on pins DIO BC-0.

C7-C0 Port C data.

Base+15 (Read/Write) **DIO Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL

This register provides the direction control for the DIO Ports A, B, and C. To set a port's direction to output, the corresponding bit must be set to 0 while setting the bit to 1 configures the port for input. For Ports A and B, all the bits are set using 1 bit while port C is divided into two 4 bit ports whose directions can be individually set.

MODEC-A	Mode configuration bits. These must be set to 0.
DIRA	Port A Direction. 1 = Input , 0 = Output
DIRCH	Port CH Direction for C4-C7 bits. 1 = Input , 0 = Output
DIRB	Port B Direction. 1 = Input , 0 = Output
DIRCL	Port CL Direction for C0-C3 bits. 1 = Input , 0 = Output

Note: *Bit 7 must be set to 1. This indicates port configure mode in the 8255 (as opposed to bit set mode, which is not supported).*

6.3.3 Page 2 Register Definitions

This is an enhanced features page. It is only accessible when enhanced features are enabled.

Base+12 (Read/Write) **Expanded FIFO Depth:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	FT9

FT9	This bit is used when setting the FIFO threshold. See the documentation for register Base+6 for more information.

6.3.4 Page 3 Register Definitions

These registers are used to control the auto-calibration process. For user software-controlled auto-calibration, these registers are used by the Universal Driver software or the user's software to manage the calibration process.

Base+12 (Read/Write) **EEPROM/TrimDAC Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.

The TrimDAC data cannot be read back.

Base+13 (Read/Write) **EEPROM/TrimDAC Address:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	A6	A5	A4	A3	A2	A1	A0

A6-A0 EEPROM/TrimDAC address.

The EEPROM recognizes address 0 — 127 using address bits A6 — A0 of this register. The TrimDAC only recognizes addresses 0 — 7 using bits A2 — A0. In each case, remaining address bits will be ignored.

Base+14 (Write) **Calibration Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	EE_EN	EE_RW	RUNCAL	MUXEN	TDACEN	-	-	-

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM.

MUXEN Calibration multiplexor enable. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.

1 = Enable cal mux and disable user analog input channels.

0 = Disable cal mux and enable user inputs.

TDACEN TrimDAC Enable. Writing 1 to this bit initiates a transfer to the TrimDAC (used in the autocalibration process).

Base+14 (Read) **Calibration Status:**

Bit:	7	6	5	4	3	2	1	0
Name:	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0

TDBUSY TrimDAC busy indicator:
0 = User may access TrimDAC.
1 = TrimDAC is being accessed; user must wait.

EEBUSY EEPROM busy indicator:
0 = User may access EEPROM.
1 = EEPROM is being accessed; user must wait.

CMUXEN Calmux enable status:
0 = Calibration multiplexor is not currently enabled.
1 = Calibration multiplexor is enabled and may be updated.

TDACEN TrimDAC enable status:
0 = TrimDAC is not enabled.
1 = TrimDAC is enabled and may be updated.

Base+15 (Write) **Advanced Feature Access:**

Bit:	7	6	5	4	3	2	1	0
Name:	EE_ACC							

EE_ACC EEPROM access. After entering page 3 by setting the Page bits, the user must write the value 0xA5 (binary 10100101) to this register in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents. Once the page is set and this value is written, you can make unlimited reads and writes to the EEPROM without resending this key as long as you stay on Page 3.

Enable Enhanced Features:
Writing 0xA6 to this register enables all enhanced features and sets A/D FIFO depth to 1024 samples. This enhanced feature state remains in effect until explicitly disabled.

Example:
```
outp(Base+8, 0x3)       ; // Select Page 3
outp(Base+15, 0xA6)   ; // Enable enhanced features
```

Disable Enhanced Features:
Writing 0xA7 to this register disables all enhanced features. (This is the default power-on state). Any enhanced feature currently running halts and internally clears all enhanced registers to their default state. Also, the A/D FIFO depth is set to 512.

Example:
```
outp(Base+15, 0xA7)   ; Disable enhanced features
```

Base+15 (Read) **FPGA Revision Code:**

Bit:	7	6	5	4	3	2	1	0
Name:	REV							

REV This register is the revision level of the FPGA design. This value changes with new versions of the FPGA. It provides a way to distinguish between different versions of FPGA code.

6.3.5 Page 5 Register Definitions

This is an enhanced features page. It is only accessible when enhanced features are enabled.

Base+12 (Write) **Waveform Buffer Address (LSB):**

Bit:	7	6	5	4	3	2	1	0
Name:	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0

DACA7-0 LSB of address to store D/A code in D/A waveform buffer.

Base+13 (Write) **Waveform Buffer Address (MSB):**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	DACA9	DACA8

DACA9-8 MSB of address to store D/A code in D/A waveform buffer.

Base+14 (Read/Write) **Waveform Generator Control:**

Bit:	7	6	5	4	3	2	1	0
Name:	DEPTH				WGCH1	WGCH0	WGSRC1	WGSRC0

DEPTH This 4-bit parameter defines the size of the D/A waveform buffer. The depth is based on this equation:

Depth = [(DEPTH) + 1] * 64

This allows valid depth values from 64 to 1024 samples.

The waveform generator frame pointer will return to 0 whenever it hits either 1024 or the depth value indicated above.

WGCH1-0 These two bits combine to choose how many codes are output on each frame.

WGCH1	*WGCH0*	*Description*
0	0	One code per
0	1	Two codes per
1	X	Four codes per

WGSRC1-0 These two bits combine to choose which trigger source is used to increment the waveform by one frame.

WGSRC	*WGSRC0*	*Description*
0	0	Manual (using WGINC)
0	1	Counter 0 output
1	0	Counter 1/2 output
1	1	External trigger (J31, pin 31)

Base+15 (Write) **Waveform Generator Command:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	WGINC	WGRST	WGPS	WGSTRT

WGINC Begin or resume the waveform generator.

WGRST Pause/stop the waveform generator. The current position in memory is saved for the next begin/resume, or can be reset using WGRST.

WGPS Reset the waveform generator to output from the beginning of the D/A code buffer.

WGSTRT Force the waveform generator to increment one frame.

Note: Only one bit can be set to 1 at a time. Bits are processed from the MSB to the LSB. The first 1 bit determines which command is executed.

6.3.6 Registers 16-23

The registers Base+16 to Base+23 exist only on Page 0 of the register map.

Base+16 (Read/Write) **Address Pointer/Enable:**

Bit:	7	6	5	4	3	2	1	0
Name:	ENABLE	-	-	-	A3	A2	A1	A0

ENABLE Enables chip selects for the 8 serial ports.
0 = disable
1 = enable
On power-up or reset, all ports are automatically programmed from the EEPROM and enabled. For more information regarding the EEPROM, please refer to Section 11 of this document.
When manually programming the address and IRQ registers, this bit must be set after programming is complete in order to enable the serial ports.

A3-A0 Address of internal configuration register:
0–3 Address registers for ports COM3–COM6, respectively.
4–7 Interrupt level register for ports COM3–COM6, respectively.
8 Protocol register for ports COM3–COM6.

Base+17 (Write) **Data for Address/IRQ No.:**

Bit:	7	6	5	4	3	2	1	0
Name:	-	D6	D5	D4	D3	D2	D1	D0

D6-D0 For address registers, D6–D0 contains the upper seven bits of the 10-bit base address of the serial port. Valid port base addresses are 0x100 to 0x3F8.
For interrupt level registers, Only D3–D0 are used. Valid values are 2, 3, 4, 5, 6, 7, 10, 11, 12, and 15. Any other value prevent interrupts from operating on the selected port.

For example:

Desired I/O address = 140 Hex = 0 1 0 1 0 0 0 0 0
Only the upper 7 bits are needed. The three lowest bits are always 0, resulting in all addresses being on 8-byte boundaries.
Necessary bits = 0 1 0 1 0 0 0 = 28 Hex
An easy way to generate these bits is to divide the I/O address by 8 or shift right 3 places.

Base+17 (Read) **Address Read-back:**

Bit:	7	6	5	4	3	2	1	0
Name:	ADDRESS							

ADDRESS This register provides a means to read back the current address settings for Ports 1–4 (COM3-COM6) as a diagnostic tool to verify that the board is present and responding. Using this technique, all 4 address registers can be read back, but the IRQ registers cannot be read back. All 9 register values can be read back from the EEPROM.

Interrupt Status: Base+18 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	INT3	INT2	INT1	INT0

INT3-INT0 Indicates the status of each port's interrupt request line. The register operates regardless of whether or not interrupt sharing is enabled. If two or more ports are sharing the same interrupt level, the status register indicates the correct status of each port's interrupt request line. If different ports are sharing different interrupt levels, the status register continues to operate correctly.

Status of interrupt request for each port:

0 = No interrupt request active.

1 = Interrupt request active.

Base+19 (Write) **Optoisolated Output Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	OPTO_I7	OPTO_I6	OPTO_I5	OPTO_I4	OPTO_I3	OPTO_I2	OPTO_I1	OPTO_I0

OPTO-10 –OPTO_I7 Optoisolated I/O input data

Optoisolated Output Data Read-back: Base+19 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	OPTO_I7	OPTO_I6	OPTO_I5	OPTO_I4	OPTO_I3	OPTO_I2	OPTO_I1	OPTO_I0

OPTO-10 –OPTO_I7 Optoisolated I/O input data

Base+20 (Write) **EEPROM Command and Address:**

Bit:	7	6	5	4	3	2	1	0
Name:	R/W	EEA6	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0

R/W Read/Write command:
1 = Write operation.
0 = Read operation.

EEA6-EEA0 EEPROM address. The EEPROM has 256 bytes, of which only the lowest 64 are accessible. The lowest 16 contain configuration information for the board. The other registers are available for customer application.

This register is used to initiate an EEPROM read or write operation. To initiate the operation, first the data are written to Base+21 and then the address and read/write bit are written to this register. After starting the operation, the application program should monitor the BUSY bit by reading this address to know when the operation is complete.

Base+20 (Read) **EEPROM Busy Status:**

Bit:	7	6	5	4	3	2	1	0
Name:	BUSY	---						

BUSY The Busy bit indicates whether the EEPROM is busy with a read, write, or reload operation. The application program must monitor this bit after each read, write, or reload operation before proceeding to another one. If a new EEPROM operation is commenced without waiting for the previous one to complete, the new operation is ignored.
1 = Busy.
0 = Idle.

Base+21 (Read/Write) **EEPROM Data:**

Bit:	7	6	5	4	3	2	1	0
Name:	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0

EED7-EED0 When writing to the EEPROM, the data is first written to this register before the address and write bit are written to Base+20.
When reading from the EEPROM, the address to read from is first written to Base+20. The program must then monitor the BUSY bit in Base+20. When the BUSY bit is 0, the program may read valid EEPROM data from this register.

Base+22 (Write) **Reload Command:**

Bit:	7	6	5	4	3	2	1	0
Name:	RELOAD	---						

RELOAD Set the RELOAD bit to 1 to force a reload of the eight address settings and eight interrupt level settings from the EEPROM into the board. The BUSY bit (Base+20, bit 7) goes high and stays high until the reload is complete.

This register is used to cause a reload of the contents of the EEPROM into the board's configuration registers. This can be done at any time. For example, RELOAD can be used to recall known good settings should the user loads invalid data into the registers.

Note: *Register Base+23 is not used.*

6.3.6.1 Serial port registers accessed using Base+16 and Base +17

The Neptune baseboard contains nine additional registers for selecting the address and interrupt level for serial ports COM3 – COM6. These registers are accessed indirectly through the address pointer register at Base+16. The register map is shown below:

Register No.	Function
0	COM3 Address
1	COM4 Address
2	COM5 Address
3	COM6 Address
4	COM3 IRQ No.
5	COM4 IRQ No.
6	COM5 IRQ No.
7	COM6 IRQ No.
8	COM1-4 Protocol Configuration

The following considerations apply to the use of these registers:

- To write data to a register — first write the number of that register (0 — 8) to the board's address pointer/enable register at Base address + 16. Then write the data to the board's data register at Base address + 17.
- To program an address for a port — write the upper 7 bits of the 10 bit I/O address into bits 6 — 0 of the address register for that port. The value written to the address register is therefore the desired I/O address divided by 8. All I/O addresses should be on 8 byte boundaries between 100 Hex and 3F8 Hex. Addresses below 100 Hex are reserved for CPU functions. A value of 00 Hex for a port address will disable that port.
- To select an interrupt level for a port — write the desired interrupt level to that port's interrupt level register. Valid interrupt levels are 3, 4, 5, 6, 7, 9, 10, 11, 12, and 15. Writing any other value to the interrupt level register including 00 Hex will cause that port not to generate interrupts.

Bit 7 of Base address + 16 is the port enable bit (ENABLE) and must be set after manual loading of port addresses and interrupts in order to enable serial port operation. On power-up or reset, all ports are automatically reloaded with the EEPROM values and then enabled.

To configure the serial protocol for each port the pair of bits assigned to that port must be configured as shown below:

REGISTER # 8

Bit No.	7	6	5	4	3	2	1	0
Name	COM4 CFG1	COM4 CFG0	COM3 CFG1	COM3 CFG0	COM2 CFG1	COM2 CFG0	COM1 CFG1	COM1 CFG0

CFG1	CFG0	PROTOCOL
0	0	RS-232
0	1	RS-422
1	0	RS-485 with Echo
1	1	RS-485 without Echo

7. ANALOG I/O OPERATION

7.1 A/D Input Ranges and Resolution

The Neptune baseboard uses a 16-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is $2^{16} - 1$, so the full range of numerical values that you can get from a Neptune baseboard analog input channel is 0 - 65535.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of one in the A/D code, and is referred to as one Least Significant Bit (1 LSB).

7.2 Unipolar and Bipolar Inputs

The Neptune baseboard can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. The full-scale input voltage range depends on the Gain, Range, and Polarity bit settings in the Analog Configuration register (Base+11). In front of the A/D converter is a programmable gain amplifier that multiplies the input signal before it reaches the A/D. This gain circuit has the effect of scaling the input voltage range to match the A/D converter for better resolution. In general, you should select the highest gain possible that will allow the A/D converter to read the full range of voltages over which your input signals varies. If the gain is too high, the A/D converter clips at either the high end or low end, and you will be unable to read the full range of voltages on your input signals.

7.3 Ranges and Resolutions

The table below lists the full-scale input range for each valid analog input configuration. The parameters Polarity, Range and Gain are combined to create the value "Code", which is written to the Analog Configuration register (Base+11) to get the input range shown. A total of nine different input ranges are possible. The range programming codes 4, 5, 6, and 7 are invalid and that range codes 9–11 are equivalent to range codes 0–2.

Polarity	*Range*	*Gain*	*Code*	*Input Range*	*Resolution (1 LSB)*
Bipolar	5V	1	0	± 5V	153µV
Bipolar	5V	2	1	± 2.5V	76µV
Bipolar	5V	4	2	± 1.25V	38µV
Bipolar	5V	8	3	± 0.625V	19 µV
Unipolar	5V	1	4		Invalid Setting
Unipolar	5V	2	5		Invalid Setting
Unipolar	5V	4	6		Invalid Setting
Unipolar	5V	8	7		Invalid Setting
Bipolar	10V	1	8	± 10V	305µV
Bipolar	10V	2	9	± 5V	153µV
Bipolar	10V	4	10	± 2.5V	76µV
Bipolar	10V	8	11	± 1.25V	38µV
Unipolar	10V	1	12	0-10V	153µV
Unipolar	10V	2	13	0-5V	76µV
Unipolar	10V	4	14	0-2.5V	38µV
Unipolar	10V	8	15	0-1.25V	19 µV

7.3.1 Conversion Formulas

The 16-bit value returned by the A/D converter is always a two's complement number ranging from -32768 to 32767, regardless of the input range. This is because the input range of the A/D is fixed at ±10V. The input signal is actually magnified and shifted to match this range before it reaches the A/D. For example, for an input range of 0–10V, the signal is first shifted down by 5V to ±5V and then amplified by two to become ±10V. Therefore, two different formulas are needed to convert the A/D value back to a voltage, one for bipolar ranges, and one for unipolar ranges.

To convert the A/D value to the corresponding input voltage, use the following formulas, depending on bipolar or unipolar mode of operation.

7.3.1.1 Conversion Formula for Bipolar Input Ranges

Input voltage = A/D code / 32768 * Full-scale input range

Example:

Given, Input range is ± 5V and A/D code is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The following table shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage):

A/D Code	***Input Voltage Symbolic Formula***	***Input Voltage for ±5V Range***
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

7.3.1.2 Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D code + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0–10V and A/D code is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 10V = 7.7103V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The following table illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for 0-5V Range*
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.153 mV
...	...	...
-1	V_{FS} / 2 - 1 LSB	4.99985V
0	V_{FS} / 2	5.0000V
1	V_{FS} / 2 + 1 LSB	5.00015V
...	...	...
32767	V_{FS} - 1 LSB	9.9998V

7.4 A/D Sampling Methods

7.4.1 Sampling Modes

There are several different A/D sampling modes available on a Neptune baseboard. The desired mode is selected with the FIFOEN and SCANEN bits at the FIFO Control register (Base+7), and the ADINTE bit in the Interrupt Control register (Base+9).

> ***Note:*** *If interrupts are not enabled, the FIFO should not be enabled. FIFO storage is only useful when interrupts are used. Otherwise, the FIFO has no effect.*

All of these features may be selected as arguments to function calls in the driver software. The control register details are provided for completeness and for programmers not using the driver.

SCANEN	***FIFOEN***	***ADINTE***	***Mode***	***Description***
No	No	No	Single Conversions	The most basic sampling method. Used for low-speed sampling (typically up to about 100 Hz) under software control where a precise rate is not required, or under external control where the rate is slow. Consists of either one channel or multiple channels sampled one at a time.
Yes	No	No	Scan Conversions	Used to sample a group of consecutively numbered channels in rapid succession, under software or external control. The time between samples in a scan is programmable between 5 to 20 microseconds, while the time between scans depends on the software or external trigger and may be very short or very long, but is usually less than about 100 Hz (above this rate use interrupt scans below).
No	No	Yes	Interrupt Single Conversion, Low Speed	Used for controlled-rate sampling of single channels or multiple channels in round-robin fashion, where the frequency of sampling must be precise but is relatively slow (less than 100 Hz). The sampling clock comes from the on-board counter/timer or from an external signal. The interval between all A/D samples is identical.
Yes	No	Yes	Interrupt Scans, Low Speed	Used for controlled-rate sampling a group of channels in low-speed mode (less than 500 Hz per channel). Each sampling event consists of a group of channels sampled in rapid succession. The time between scans is determined by the sample rate.
No	Yes	Yes	Interrupt Single Conversions, High Speed	Intended for medium- to high-speed operation (recommended above about 500 Hz). Can support sampling rates up to the board's maximum of 250,000 Hz. May also be used at slower rates if desired. The sampling clock comes from the on-board counter/timer or from an external signal.
Yes	Yes	Yes	Interrupt Scan Conversions	Used for high-speed sampling of a group of channels where the scan rate is high. The sampling clock comes from the on-board counter/timer or from an external signal.

7.4.2 FIFO Description

The Neptune baseboard uses a 1024-sample FIFO (First In First Out) memory buffer to manage A/D conversion data. The FIFO is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the user program. In enhanced mode, the entire 1024-sample FIFO is available. In normal mode only 512 samples are available. The FIFO may be enabled and disabled under software control.

In single-conversion mode, the FIFO features are not generally needed so FIFO use should not be selected (although the FIFO is actually being used). Each A/D sample is stored in the FIFO. When the software reads the data, it reads it out of the FIFO. In low-speed sampling, each time a conversion occurs, the program reads the data, so there is always a one-to-one correspondence between sampling and reading. Thus, the FIFO contents never exceed one sample.

For high-speed sampling or interrupt operation, the FIFO significantly reduces the amount of software overhead in responding to A/D conversions. Using the FIFO also reduces the interrupt rate on the bus because it enables the program to read multiple samples at a time. In addition, the FIFO is required for sampling rates in excess of the maximum interrupt rate possible on the bus. Generally, the fastest sustainable interrupt rate on the ISA bus running DOS is around 40,000 per second. Since the Neptune baseboard can sample up to 250,000 times per second, the FIFO is needed to reduce the interrupt rate at high speeds. When the interrupt routine runs, it reads multiple samples from the FIFO. The interrupt rate is equal to the sample rate divided by the number of samples read each interrupt. On Neptune, this number is programmable using the FIFO Threshold register (Base+6). The usual value is 1/2 the maximum FIFO depth, or 512 samples. Therefore, the maximum interrupt rate for Neptune is reduced to 488 per second, which is easily sustainable on any popular operating system.

> ***Note:*** *If both scan and FIFO operations are enabled, the interrupt occurs at the programmed FIFO threshold and the interrupt routine reads the indicated number or samples and then exits. This happens even if the number of samples is not an integral number of scans. For example, if you have a scan size of 10 and a FIFO threshold of 256, the first time the interrupt routine runs, it reads 256 samples, consisting of 25 full scans of all 10 channels followed by 6 samples from the next scan. The next time the interrupt routine runs, it reads the next 256 samples, consisting of the remaining 4 samples from the last scan it started to read, the next 25 full scans of 10 samples, and the first 2 samples of the next scan. (If you are using the Universal Driver software, this continues until the interrupt routine ends in either one-shot or recycle mode. In one-shot mode, the last time the interrupt routine runs it reads the entire contents of the FIFO, making all data available.)*

7.4.3 Scan Sampling

A scan is defined as a quick burst of samples of multiple consecutive channels. For example, you may want to sample channels 0–15 at one time, and repeat the operation each second, resulting in a scan at a frequency of 1 Hz. Each time the A/D clock occurs (software command, timer, or external trigger), all 16 channels are sampled in high-speed succession. There is a short delay of 4–20 microseconds between each sample in the scan. Since each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate, and the total sampling rate is the programmed sampling rate times the number of channels in the scan range.

Scan sampling is independent of FIFO operation, and can be enabled independently.

7.4.4 Sequential Sampling

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. If the channel range is set to more than one channel (high channel > low channel), then the channel counter increments to the next channel in the range, and the next conversion is performed on that channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Since each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the channel range.

7.5 A/D Conversion

This section describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software).

All A/D conversions are stored in an on-board FIFO (first in first out memory). The FIFO can hold up to 1024 samples. Each time an A/D conversion is finished, the data is stored in the FIFO and the FIFO counter increments by 1. Each time you read A/D data, you are actually reading it out of the FIFO and the FIFO counter decrements by 1. When the FIFO is empty, the data read from it is undefined; you may continue to read the last sample, or you may read all 1s.

You can either read each A/D sample when they become available, or you can wait for a collection of samples (up to 1024 maximum) and read all of the samples at once.

To be sure that you are getting only current A/D data, always reset the FIFO before you start an A/D operation. This prevents errors caused by leaving data in the FIFO from a previous operation. To reset the FIFO, write a 1 to the FIFORST bit of the FIFO Control register (Base+7). This bit is not a real register bit, but it triggers a command in the board's controller chip; therefore, you do not need to write a 1 followed by a 0.

```
outp(Base+7, 0x02); // resets the FIFO and clears SCANEN and FIFOEN
outp(Base+7, 0x0A); // resets the FIFO and SCANEN but leaves FIFOEN set
```

Note: *writing to the FIFORST bit also affects the values of other bits in this register.*

This register also contains a FIFO enable bit, FIFOEN, which only has meaning during A/D interrupt operations. The FIFO is always enabled and is always in use during A/D conversions.

Perform an A/D conversion according to the following steps:

- Select the input channel
- Select the input range
- Wait for analog input circuit to settle
- Initiate an A/D conversion
- Wait for the conversion to finish
- Read the data from the board
- Convert the numerical data to a meaningful value

Each of these steps is discussed in detail, below.

The control registers associated with A/D conversions are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
0	W	STARTAD							
0	R	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	R	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	R/W	-	-	-	L4	L3	L2	L1	L0
3	R/W	-	-	-	H4	H3	H2	H1	H0
8	R	**STS**	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
11	W	**-**	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0
11	R	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0

STARTAD	Writing any value to this register will trigger an AD conversion
AD15-0	A/D data value
L3-L0	Low channel of selected A/D range (0–31)
H3-H0	High channel of selection A/D range (0–31)
STS	AD conversion status bit. 0 = A/D is idle, 1 = A/D is busy, must wait for completion.
WAIT	A/D circuit settling indicator. 0 = circuit is idle, 1 = A/D is busy.

If you are going to sample the same channel multiple times or sample multiple consecutive channels with the same input range, you only need to perform steps 1–3 once, and then you can repeat steps 4-6 or 4-7 as many times as desired.

7.5.1 Select the Input Channel

The Neptune baseboard contains a channel counter circuit that controls which channel is sampled on each A/D conversion command. The circuit uses two channel numbers called the low channel and high channel. These are stored in the A/D Low Channel and A/D High Channel registers (Base+2 and Base+3). The circuit starts at the low channel and automatically increments after each A/D conversion until the high channel is reached. When an A/D conversion is performed on the high channel, the circuit resets to the low channel and starts over again. This behavior enables you simplify your software by setting the channel range just once.

To read continuously from a single channel, write the same channel number to both the low channel and high channel registers.

To read from a series of consecutively numbered channels, write the starting channel to the A/D Low Channel register (Base+2) and the ending channel to the A/D High Channel register (Base+3).

To read from a group of non-consecutive channels, you must treat each as a single channel, as described above.

For example: To select channels 0–31 for the operation…

```
outp(base+2, 0x00) ;
outp(base+3, 0x1F) ;
```

7.5.2 Select the Input Range

Select the code corresponding to the desired input range and write it to the RANGE bit of the Analog Configuration register (Base+11). You only need to write to this register if you want to select a different input range from the one used for the previous conversion. If all channels are using the same input range, you can configure this register just once at the beginning of your procedure.

You can read the current value of this register by reading from the analog Configuration register (Base+11).

```
outp(base+11, 0x00) ; // 5V, BIPOLAR, GAIN = 1

outp(base+11, 0x0E) ; // 10V, UNIPOLAR, GAIN = 4
```

7.5.3 Wait for Analog Input Circuit to Settle

After changing either the input channel or the input range, you must allow the circuit to settle on the new value before performing an A/D conversion. The settling time is long compared to software execution times, so a timer is provided on board to indicate when it is safe to proceed with A/D sampling. The WAIT bit in the Analog I/O Read-back register (Base+11) indicates when the circuit is settling and when it is safe to sample the input. When WAIT is 1, the board is settling. When WAIT is 0, the board is ready for an A/D conversion.

```
while ( inp ( base+11) & 0x80 ); // wait for AD to be available
```

7.5.4 Perform an A/D Conversion on the Current Channel

To start an A/D conversion, simply write to the A/D Start Conversion register (Base+0). Any value may be written to the register.

```
outp(base, 0xFF) ; // trigger an AD conversion
```

7.5.5 Wait for the Conversion to Finish

The A/D converter takes about four microseconds to complete a conversion. If you try to read the A/D converter data immediately after starting a conversion, you will read invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This signal can be read back as the STS bit in the A/D Status register (Base+8). When the A/D converter is busy (performing an A/D conversion) the STS bit is 1. When the A/D converter is idle (conversion is done and data is available) the STS bit is 0.

```
while ( inp ( base + 8 ) & 0x80 ); // wait for AD conversion to end
```

7.5.6 Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is 16 bits wide and is read back in two 8-bit bytes from the A/D LSB and A/D MSB registers (Base+0 and Base+1). The low byte, A/D LSB register, must be read first.

Note: *Reading data from an empty FIFO returns unpredictable results.*

The following pseudo-code illustrates how to read and construct the 16-bit A/D value with 8-bit accesses:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

Alternatively, the value can be read as one 16-bit value, which is preferred since this method increases overall system bandwidth while reading data from the FIFO. For example:

```
Data = inpw(base); // Where the MSB and LSB are read in one access
```

The final data ranges from 0 to 65535 (0 to 256 - 1) as an unsigned integer. This value must be interpreted as a signed integer ranging from -32768 to +32767.

As noted above, all A/D conversions are stored in an on-board FIFO, which can hold up to 1024 samples in enhanced mode or 512 samples in normal mode. Whenever you read A/D data you are actually reading it out of the FIFO. Therefore, you can read each A/D sample as soon as it is ready, or you can wait until you take a collection of samples (up to 1024 maximum) and then read them all out in sequence.

7.5.7 Convert the numerical data to a meaningful value

The conversion formulas, above, describe how to convert the data back to the original input voltage. You may also convert the result into engineering units. The two conversions can be done sequentially, or the formulas can be combined into a single formula.

7.5.8 A/D Conversion Using Interrupts

Neptune can generate hardware interrupts to manage A/D conversions. Interrupt-based A/D conversions are used in several situations.

- High-speed sampling.
- Applications that need a precise sampling rate.
- Applications that base the sampling rate on an external clock.

The Universal Driver functions *dscADSampleInt()* and *dscADSetSettings()* manage all of the required parameters to generate interrupt-based A/D conversions. Below is a checklist to help you configure the function call properly. All parameters are passed in the data structure of type *DSCAIOINT* for function *dscADSampleInt()* except for the input range.

A/D channel range (low channel, high channel).

On Neptune, the channel numbers range from 0 to 31. Some channel numbers may not be available, depending on the single-ended/differential configuration mode as explained on page 11. During interrupt-based A/D conversions, the channels being sampled must be consecutive in number. To sample only a single channel, set the low channel and high channel to the same channel number. To sample a range of channels, set the low and high channels accordingly.

Input voltage range.

During interrupt-based A/D conversions, the input voltage range must be the same for all channels. Select the input range from the list of codes found in the Analog Input Ranges and Resolution section of this document. This parameter is set with the function *dscADSetSettings()* prior to calling *dscADSampleInt()*.

A/D Clock source, internal or external.

For internal clocking, the on-board 32-bit counter/timer is programmed to the desired sample rate. For external clocking, the signal EXTCLK/IN3 on connector J31, pin 31, controls sampling. Falling edges on this pin generate A/D conversions. The signal is edge sensitive; holding it low generates one conversion.

A/D conversion rate, if using internal clock.

If internal clocking is selected, provide the desired sample rate in Hz as a floating value. The maximum sample rate is 250,000 per second (maximum A/D operating speed), and the slowest rate is .000024383 Hz (100 KHz input / 232), or approximately 1 sample every 42,950 seconds (approximately 11.9 hours).

External gating enable.

You may choose to allow an external signal, EXTGATE, on connector J31, pin 32, to control the sampling. When the signal is high, sampling occurs, and when it is low, sampling pauses. External gating works with both internal and external clocking. This pin is connected to a 4.7K pull-up resistor.

One-shot vs. recycle mode (when using the Universal Driver APIs).

In one-shot mode, the operation occurs one time and then stops, and the parameter *num_*conversions determines the number of samples taken. In recycle mode, the operation runs repeatedly until you stop the operation by calling *dscCancelOp()*. In this case, the parameter *num_*conversions indicates the size of the memory buffer or array used to store the samples. Once the buffer is filled, the data is stored starting at the beginning again, causing the old data to be overwritten. In this situation, you only have access to the latest number of samples equal to *num_*conversions, and you must read the data out of the buffer before it is overwritten. The function *dscGetStatus()* can be used to indicate the current buffer position, which is the location at which the next data value will be stored.

7.6 D/A Conversion

Neptune uses a 4-channel 12-bit D/A converter (DAC) to provide four analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, so the full range of numerical values that the DACs support is 0–4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve.

The control registers associated with D/A conversions are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
4	W	**DA7**	**DA6**	**DA5**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**
4	R	**DACBUSY**	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0
5	W	**DACH**		**DASIM**	DAGEN	**DA11**	**DA10**	**DA9**	**DA8**

DA7-0 D/A bits 7-0. DA0 is the LSB.

DA11-8 D/A bits 11-8. DA11 is the MSB.

DACH Channel numbers 0-3.

DACBUSY Indicates that DAC is busy updating. 1 = Busy, 0 = Idle.

DASIM D/A simultaneous mode. 0 = Immediate update, 1 = Simultaneous update.

Note: *In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from Neptune's computer hardware to an analog signal terminating at an external source.*

7.6.1 Resolution

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is 1/(2^{12}), or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB). The value of this LSB is calculated as follows.

1 LSB = Output voltage range / 4096

The maximum voltage swing is defined as the difference between the highest nominal output voltage and the lowest output voltage. For an output range of 0-10V or +/-5V, the maximum voltage swing is 10V.

Example:

For, Output range = +/- 5V;

Maximum voltage swing = 10V

Therefore,

1 LSB = 10V / 4096 = 2.44 mV

7.6.2 Full-scale Range Selection

The D/A converter chip on Neptune requires two references, one for the low end and one for the high end of the range. The high end can be set to 5V, 10V, or Programmable, and the low end can be either 0V (for unipolar output ranges) or minus the high-end voltage. All channels are set to the same output range.

On power-up, the D/A automatically resets to mid-scale, which is 0V in bipolar mode and 1/2 full-scale voltage in unipolar mode.

7.6.3 Performing a D/A Conversion

This section describes the steps involved in generating an analog output on a selected output channel using direct programming, without the driver software.

Perform a D/A conversion according to the following steps. Each step is discussed in detail in the following section.

- Compute the D/A output value for the desired output voltage.
- Compute the LSB and MSB values.
- Add the channel number to the MSB.
- Set D/A Simultaneous Update bit.
- Write the LSB and MSB to the board.
- Monitor the DACBUSY status bit.

7.6.3.1 Compute the D/A Output Value for the Desired Output Voltage

A different formula is required for bipolar and unipolar output ranges.

Note: The DAC cannot generate the actual full-scale reference voltage, which would require an output code of 4096 that is not possible with a 12-bit number. The maximum output value is 4095. Therefore, the maximum possible output voltage is 1 LSB less than the full-scale reference voltage.

Unipolar Mode D/A Formula

Output value = (Output voltage) / (Full-scale voltage) * 4096

Example:

Desired output voltage = 2.168V, full-scale voltage = 5V, unipolar mode (0–5V)

Output code = 2.168V / 5V * 4096 = 1776

Bipolar Mode D/A Formula

Output value = (Output voltage) / (Full-scale voltage) * 2048 + 2048

Example:

Desired output voltage = -2.168V, full-scale voltage = 5V, bipolar mode (±5V)

Output code = -2.168V / 5V * 2048 + 2048 = 1160

7.6.3.2 Compute the LSB and MSB Values

Use the following formulas to compute the LSB and MSB values:

LSB = (D/A Code) AND 255. Keep only the low 8 bits.

MSB = int((D/A code) / 256). Strip off low 8 bits, keep 4 high bits.

Example:

Output code = 1776

LSB = 1776 AND 255 = 240 (F0 Hex)

MSB = int(1776 / 256) = int(6.9375) = 6

(In other words, 1776 = 6*256 + 240)

7.6.3.3 Add the Channel Number to the MSB

Write the channel number, 0-3, to the DAC MSB + Channel register(Base+5) DACH bits.

Example:

MSB = MSB + Channel * 64

7.6.3.4 Set D/A Simultaneous Update Bit

To update the DAC, set the DAC MSB + Channel register (Base+5) DASIM bit to 0. This performs an update of the current channel and all previously latched channels, causing a simultaneous update. If no other channels were previously latched, this only updates the current channel. To latch the channel set DASIM bit to 1.

Update example:

MSB = MSB & 0xDF

Latch example:

MSB = MSB + 32

7.6.3.5 Write the LSB and MSB to the Board

Write the LSB to the DAC LSB register (Base+4) and write the MSB/channel no. to the DAC MSB + Channel register (Base+5).

Note: If you are using enhanced features be sure to also enable enhanced features before writing to the registers, by setting the DASIM and DAGEN bits as needed.

```
outp(base+4, LSB) ;
outp(base+5, MBS) ; // MSB + CHANNEL  will update the D/A output
```

7.6.3.6 Monitor the DACBUSY Status Bit

The Status/Auxiliary Digital Inputs register (Base+4) DACBUSY bit is 1 for 10 us, while the data in the LSB and MSB registers are serially shifted into the D/A chip. After DACBUSY returns to 0 you can again write to the LSB and MSB register; the data registers should NOT be written to while DACBUSY is 1. When updating multiple channels for simultaneous update, repeat steps 1 to 6 as shown in the following example.

Compute D/A code.

Using the bipolar mode formula, we compute D/A code = 3V / 5V * 2048 + 2048 = 3276.8.
Round this up to 3277. (Binary value = 1100 1100 1101)

Compute LSB and MSB.

LSB = 3277 & 255 = 205 (Binary value = 1100 1101)
MSB = int(3277/256) = 12 (Binary value = 1100)

Add channel number to MSB.

MSB = 12 + 1 * 64 = 76

Check DASIM. For non-simultaneous update DASIM = 0, for latching DASIM = 1.

To update: MSB = MSB & 0xDF

To latch: MSB = MSB + 32

Write LSB and MSB to board, enable enhanced features if using latching.

```
outp(Base + 8, 3);     //select page 3
outp(Base + 15, 0xA6); //enable enhanced features
outp(Base + 4, LSB);
outp(Base + 5, MSB);
```

Monitor DACBUSY bit in the Status/Auxiliary Digital Input register (Base + 4).

```
while (inp(Base + 4) & 0x80);
```

7.7 Waveform Generator

The I/O map Page 5 registers provide D/A waveform generator control. The D/A waveform generator uses an in-FPGA memory block of 1024 words to store D/A codes. The FPGA parses through this memory at a user-programmable speed (or using a manual/external trigger) while sending codes to the D/A converter. The generator automatically stops if enhanced features are disabled.

The generator works on frames. A new frame is triggered from a programmable source (manual, counters, external, etc.). For each frame, the FPGA sends a programmable (1, 2 or 4) number of D/A codes from the generator's memory bank to the DAC. This transfer is done in latched mode and the DAC is updated after all codes in a frame are sent. The generator continues this process, incrementing through the memory until it reaches the end of the buffer or reaches a programmable depth, where it wraps back to the beginning of the buffer and continues operation. The generator can be paused, resumed or reset to the beginning of the memory bank at any time.

With the use of the memory block the D/A waveform generator can output consistent waveforms at a maximum frequency of 100 KHz. There are four different input sources available for the D/A waveform generator.

- Manual software trigger
- Counter 0 output
- Counters 1+2 output
- External trigger

The memory block depth is programmable from 64 to 1024 and is programmable in multiples of 64. When the programmed depth is reached, the data wraps to the beginning of the buffer.

The control registers associated with waveform generation are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
4	W	**DA7**	**DA6**	**DA5**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**
4	R	**DACBUSY**	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0
5	W	**DACH**	DASIM	**DAGEN**	**DA11**	**DA10**	**DA9**	**DA8**	
Page 5 : (Enhanced Features only)									
12	W	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
13	W	-	-	-	-	-	-	DACA9	DACA8
14	R/W	**DEPTH3**	**DEPTH2**	**DEPTH1**	**DEPTH0**	**WGCH1**	**WGCH0**	**WGSRC1**	**WGSRC0**
15	W	**-**	**-**	**-**	**-**	**WGINC**	**WGRST**	**WGPS**	**WGSTRT**

DACA7-0	LSB of address to store D/A code in D/A buffer
DACA9-8	MSB of address to store D/A code in D/A buffer
DEPTH3-0	4 bit depth value of waveform buffer
WGCH1-0	Number of codes to output in each frame
WGINC	Increment by one frame
WGRST	Reset the waveform generator
WGPS	Pause/Stop the waveform generator
WGSTRT	Begin or resume waveform generator

7.7.1 Programming the D/A Waveform Generator

This section describes how to program the D/A waveform generator through direct I/O without using the driver software.

> ***Note:*** *The D/A waveform generator is an enhanced feature. Use of this feature requires enhanced features to be enabled as described below.*

Program the D/A waveform generator using the following steps (register Page 5 must be selected):

- Enable enhanced features
- Reset D/A waveform pointer
- Latch D/A value
- Store D/A values into buffer
- Setup D/A waveform settings
- Start D/A waveform generator

7.7.2 Enable Enhanced Features

Enable enhanced features is described in the Enabling Enhanced Features section of this document.

7.7.3 Reset D/A Waveform Pointer

Reset the D/A waveform pointer by writing a 1 to the WGPS bit of the Waveform Generator Command register (Base+15). This causes the pointer to start at the beginning, address 0.

7.7.4 Latch D/A Value

The D/A value code must be computed for the desired voltage. From the computed value, obtain the LSB and MSB. To the MSB byte, add the channel number and set DAGEN bit, as shown in the DAC MSB +channel register (Base+5). By setting the DAGEN bit to 1, the D/A value written will be latched to internal memory instead of the DAC chip. Write final the LSB and MSB to the DAC LSB and DAC MSB + Channel registers (Base+4 and Base+5).

7.7.5 Store D/A Values into Buffer

Once the D/A code is latched, it must be stored in the waveform buffer. Write the buffer address (0 to 1023) for the latched D/A value into the Waveform Buffer Address registers, LSB and MSB (Base+12 and Base+13). When the MSB is written, the latched D/A value at the DAC LSB and DAC MSB + Channel registers (Base+4 and Base+5) is loaded and stored into the waveform memory. Both the D/A output code and the D/A output channel are stored.

7.7.6 Setup D/A Waveform Settings

D/A waveform settings include input source, number of code per frame and threshold. Each can be individually set, in any combination.

There are four different input sources from which to choose:

- manual/software trigger
- counter 0 output
- counters 1+2 output
- external trigger

Manual trigger should be used when the rate is slow or inconsistent and needs be controlled in software. Counter 0 output should be used when a consistent rate is desired and counter 1/2 is used for A/D interrupts. Counter 1+2 should be used when a consistent rate is desired and counter 0 is used for other interrupt functions, or if you want to synchronize the waveform generator to A/D interrupt functionality. External trigger should be used when an external signal is desired to generate D/A waveform.

Input source is set on using the Waveform Generator Control register (Base+14) WGSRC0 and WGSRC1 bits.

The number of the code per frame determines the number of buffer values that will be output per frame. Each code is determined by the value set at its address.

For example, if the codes per frame option is set at 2, the first frame will output the codes at address 0 and 1, then 2 and 3, then 4 and 5 and so on.

The number of the code per frame is set using the Waveform Generator Control register (Base+14) WGCH0 and WGCH1 bits.

Threshold determines the number of the code to output before the pointer starts over. The threshold must be set in multiples of 64 up to 1024. When the threshold is reached, the pointer wraps to the beginning.

Threshold is set using the Waveform Generator Control register (Base+14) DEPTH bits.

7.7.7 Start D/A Waveform Generator

Initialize D/A waveform output by writing 1 to the Waveform Generator Command register (Base+15) WGSTRT bit. The generator continues to output the periodic waveform until you disable it.

7.8 Auto-calibration

Neptune features automatic calibration of both analog inputs and outputs. The potentiometers, which are subject to tampering, vibration, and maladjustment, have been completely eliminated. Instead, all calibration adjustments are performed using an octal 8-bit TrimDAC and precision, low-drift reference voltages on the board. The optimum TrimDAC values for each input range are stored in an EEPROM and recalled automatically on power-up.

To calibrate the board through software a calibration utility program and software driver function enables you to calibrate the analog inputs and outputs at any time for any range and store the settings in the EEPROM. This feature dramatically improves the accuracy and reliability of the board, since you can calibrate the board as often as desired without worrying about temperature or time drift.

On the analog outputs, the full-scale output range is programmable to any voltage up to 10V, and the board will calibrate to the programmed range. The analog outputs are fed back to the A/D converter so that they can also be calibrated without user intervention.

7.8.1 Background

The Neptune auto-calibration circuit uses an octal 8-bit TrimDAC IC to provide small adjustments to the offset and gain at various points in the circuit. Four of the DACs are used for the A/D calibration, and the other four are used for the D/A. The 8-bit TrimDAC values are stored in an on-board EEPROM and are recalled automatically on power-up.

An on-board ultra-stable +5V reference chip with 5 ppm offset drift is used as the voltage reference for all calibration operations. From this reference several intermediate values are derived that are used for the calibration: one is just under +5V and one is just above 0V. These values are measured at the factory, and their values are stored in the on-board EEPROM for use by the calibration program. Note that the actual values of the reference signals does not matter, as long as they are stable, since the calibration routine knows the values and can adjust the calibration circuit to achieve them. An extra input multiplexor chip is used to feed the calibration voltages into the A/D circuit during the process.

For bipolar A/D calibration, first 0V is measured, and then the TrimDAC is adjusted until the target A/D reading is achieved. For unipolar calibration, the voltage just above 0 is used as the first measurement value. Two TrimDAC channels are used for the offset. The first channel provides a coarse adjustment to bring the A/D readings into range, and the second channel provides a fine adjustment for maximum accuracy. The use of both coarse and fine adjustments provides a wider range of total adjustment capability. The range of the fine adjustment exceeds the smallest change in the coarse adjustment, so there is no gap in the adjustment range.

After the offset is adjusted, the full-scale is adjusted in a similar manner. The reference value just under 5V is fed into the A/D, and two additional TrimDACs provide coarse and fine adjustments to achieve the target A/D near-full-scale reading.

Once the A/D is completely calibrated, the 12-bit D/A channels can be calibrated. Unlike the A/D circuit, which uses a single A/D for all input channels, the D/A circuit actually contains a single D/A converter for each of the four output channels. These channels are fed into the calibration multiplexor and the remaining four TrimDAC channels are used to calibrate them in a similar manner to the A/D. A single adjustment is used for the high reference, and both coarse and fine adjustments are used for the low reference.

The entire process takes a few second for each input range. Once it is complete, the board is ready to run. All eight TrimDAC values are stored in the EEPROM so that the next time power is cycled to the board, the values are loaded automatically.

7.8.2 Performing Auto-calibration with Software

The Universal Driver software (v6.00 or later) provides two functions, dscADAutocal() and dscDAAutocal() API support for Neptune board, which can be called from within a user program to calibrate the board at any time.

8. DIGITAL I/O OPERATION

Neptune contains two sets of digital I/O lines:

- An internal 82C55-type digital I/O circuit provides 24 digital I/O lines that emulate the function of Mode 0 of an 8255 chip. These lines are buffered to provide extra drive current in output mode, and are available on digital I/O connector J31. This is hereafter referred to as the "main digital I/O."
- Digital I/O header J31 also contains what will be referred to as "auxiliary digital I/O." Four inputs and three outputs can be used for general purpose DIO as long as they are not used for any special functions.

The control registers associated with Digital I/O operations are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
8	W	**-**	**-**	RESETA	RESETD	INTRST	**PG2**	**PG1**	**PG0**
12	R/W	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
13	R/W	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
14	R/W	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
15	R/W	1	MODEC	MODEA	**DIRA**	**DIRCH**	MODEB	**DIRB**	**DIRCL**

A7-0 Digital I/O port A
B7-0 Digital I/O port B
C7-0 Digital I/O port C
DIRA Port A direction: 0 = output , 1 = input
DIRB Port B direction: 0 = output , 1 = input
DIRCH Port C bits 7–4 direction : 0 = output, 1 = input
DIRCL Port C bits 3–0 direction : 0 = output, 1 = input

8.1 Main Digital I/O Internal 82C55 Circuit

The 82C55-type digital I/O circuit is accessed through Page 1 registers, Base+12 through Base+15. This means that address 0 on the chip is equivalent to address 12 in the register map. Before performing any access to the digital I/O circuit, you must set the current page to Page 1 using the Miscellaneous Control and Page register (Base+8). outp (base + 8 , 1) ; // set page bits to page 1

> ***Note:*** *Writing page bits to the Miscellaneous Control and Page register does not cause a board reset or interrupt reset operation as long as the two reset bits are left at 0. Also, writing a 1 to either reset bit in this register does not change the contents of the page bits.*

The current page may be determined by reading the PAGE bits in the FIFO Status register (Base+7).

This digital I/O circuit functions like an 82C55 in Mode 0, direct I/O, or Mode 1, latched I/O. In Mode 1, latch and acknowledge signals are provided. Each port, A, B and C, can be programmed for input or output. Port C can also be split into two halves, with each half programmed for a different direction.

All 24 lines have 10KΩ resistors connected to them that can be configured for either pull-up or pull-down operation. In addition, all lines are buffered by 74FCT245 line drivers between the controller chip and the I/O header. These line drivers change direction automatically in response to the control word written.

On power-up, all ports are set to input mode and can be used as inputs immediately. Before using any port as an output, the port direction register must be programmed appropriately.

The following table provides a list of common configuration register values for programming port direction.

Value	*Port A*	*Port B*	*Port C*
9Bh	Input	Input	Input
92h	Input	Input	Output
99h	Input	Output	Input
90h	Input	Output	Output
8Bh	Output	Input	Input
82h	Output	Input	Output
89h	Output	Output	Input
80h	Output	Output	Output

8.1.1 Mode 0 Digital I/O

This is the simpler of the two I/O modes and works well for most uses. In mode 0, the handshaking signals Latch and Acknowledge are not used. When reading any port in input mode, the data at the I/O pins at the time of the read command is returned.

8.1.2 Mode 1 Digital I/O With Handshaking

In Mode 1, a Latch input and an Acknowledge output signal are provided for handshaking operation. This allows the external circuit to tell the board when new input data is ready or when it has accepted the current output data, and it allows the board to tell the external circuit when it has read the current input data and when new output data is ready. Only Port A may be operated in Mode 1.

In all cases, the starting/resting conditions are Latch input = low, and Acknowledge output = low.

8.2 Auxiliary Digital I/O

Connector J31 has three digital outputs and four digital inputs that can be used either for general purpose digital I/O, or for A/D and counter/timer functions. The operation of these bits is controlled with various bits in two control registers.

8.2.1 Outputs

- OUT2/CTROUT2 (pin 28) — The function of this pin is determined by OUT2EN bit of the Counter/timer and DIO Control register (Base+10).
- OUT1/SHOUT (pin 30) — This pin is always the value written to OUT1 bit of the Auxiliary digital Output register (Base+1).
- OUT0/CTROUT0 (pin 27) — The function of this pin is determined by OUT0EN bit of the Counter/Timer and DIO Control register (Base+10).

8.2.2 Inputs

- IN3/EXTCLK (pin 31) — This signal may always be read from the Status/Auxiliary Digital Input register (Base+4), IN3 bit. It may function as an external clock to control A/D conversion timing when CLKEN = 1 and CLKSEL = 0, in the Interrupt and A/D Clock Control register (Base+9).
- IN2/EXTGATE (pin 32) — This signal may always be read from the Status/Auxiliary Digital Input register (Base+4), IN2 bit. It may function as an external gate to enable and disable A/D conversions when GT12EN = 1, of the Counter/timer and DIO Control register (Base+10).
- IN1/GATE0 (pin 26) — This signal may always be read from the Status/Auxiliary Digital Input register (Base+4), IN1 bit. It may function as an external gate for Counter 0 when GT0EN = 1 of the Counter/timer and DIO Control register (Base+10). When used as a gate, it is active high, which means that Counter 0 counts as long as it is high and does not count when it is low.
- IN0/CLK0 (pin 25) — This signal may always be read from the Status/Auxiliary Digital Input register (Base+4), IN0 bit. It may function as an external clock for counter 0 when SRC0 = 0 of the Counter/timer and DIO Control register (Base+10). When used as a clock for Counter 0, the rising edge is active.

8.3 Optoisolated I/O

The Neptune baseboard provides 8 optoisolated (opto) I/O lines for achieving isolation. These signals are available on connector J33. The optoisolated I/O circuit is accessed through the read/write register Base+19 in page 0.

The control registers associated with D/A conversions are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
19	R/W	**OPTO-7**	**OPTO-6**	**OPTO-5**	**OPTO-4**	**OPTO-3**	**OPTO-2**	**OPTO-1**	**OPTO-0**

OPTO7-0 Optoisolated I/O data.

8.3.1 Opto output

The opto output pins are named OUT0_OUT to OUT7_OUT on the connector J33. Each of these pins is controlled by the data in the register Base+19.

The binary value of any of the bit in the register results in an inverted logic on the corresponding opto pin on the port.

Steps for using the opto outputs:

- Connect the voltage reference (+5V - +24V DC) desired on the VCC#_OUT pin of the connector J33.
- Connect the GND of the voltage reference to the GND#_OUT pin of the connector J33.
- Connect the signal to control to the OUT#_OUT pin on the connector J33.

To output a value of 0xFF on the opto port:

```
outp( base+19, 0x00 ) ; // OUT0_OUT — OUT7-OUT all will be set to 1.
```

8.3.2 Opto input

The opto input pins are named A0_IN - A7_IN and B0_IN — B7_IN. When the register at base+19 is read, the data read is the actual state of the opto inputs.

```
opto_data = inp( base+19 ) ;
```

9. COUNTER/TIMER OPERATION

The Neptune baseboard's counter/timer circuit emulates an 82C54 counter/timer chip, providing three 16-bit counter/timers.

The control registers associated with D/A conversions are provided below for reference. The registers for counter/timer are in Page 0.

Base +	R/W	7	6	5	4	3	2	1	0
12	R/W	**CTR0D7**	**CTR0D6**	**CTR0D5**	**CTR0D4**	**CTR0D3**	**CTR0D2**	**CTR0D1**	**CTR0D0**
13	R/W	**CTR1D7**	**CTR1D6**	**CTR2D5**	**CTR1D4**	**CTR1D3**	**CTR1D2**	**CTR1D1**	**CTR1D0**
14	R/W	**CTR2D7**	**CTR2D6**	**CTR2D5**	**CTR2D4**	**CTR2D3**	**CTR2D2**	**CTR1D1**	**CTR2D0**

CTR0D7–0 Counter 0 data

CTR1D7–0 Counter 1 data

CTR2D7–0 Counter 2 data

9.1.1 Features and Configuration Options

Counters 1 and 2 are cascaded together to form a 32-bit counter/timer for use as a programmable A/D sampling clock. The output of counter 1 provides the input for counter 2, and the output of counter 2 is fed to the A/D triggering circuit as well as the I/O header J31. If not being used for A/D sampling, these counter/timers may be used for other functions. Counter/timer 0 is always available for user applications.

The inputs of the counter/timers are programmable, and the outputs may be routed to the J31 I/O header under software control. The table below lists the key features of each counter/timer.

Counter	***Input***	***Gate***	***Output***
0	• 10 MHz on-board • 10 KHz on-board • IN0/CLK0 (J31, pin 25)	IN1/GATE0 (pin 26)	OUT0/CTROUT0 (pin 27)
1	• 10 MHz • 100 KHz	IN2/EXTGATE (pin 32)	Not available
2	• Counter 1 out	IN2/EXTGATE (pin 32)	• OUT2/CTROUT2 (pin 28) • Used internally for A/D sampling control

9.1.2 Counter/Timer Configuration

The counter/timer configuration is determined by the Counter/Timer and DIO Control register (Base+10). The outputs of counters 0 and 2 are routed to pins on I/O header J31 under software control rather than being hardwired.

Configuring the A/D sampling clock is done with the Interrupt and A/D Clock Control register (Base+9). Bit CLKEN selects whether or not the A/D hardware clocking is enabled. If clocking is enabled, bit CLKSEL selects whether or not it is the output of counter/timer 2 or the external clock input at IN3/EXTCLK, on the J31 connector.

9.1.3 Counter/Timer Access and Programming

Before performing any access to the chip, you must set the current page to Page 0 with the Miscellaneous and Page Control register (Base+8) to ensure that the proper page is enabled. Note that writing page bits to the miscellaneous control register does not cause a board reset or interrupt reset operation as long as the two reset bits are left at 0. Also, writing a 1 to either reset bit in this register does not change the contents of the page bits.

The current page may be determined by reading the PAGE bits in the FIFO Status register (Base+7).

Once you write the value to select Page 0, you can read and write to the 82C54 registers.

10. WATCHDOG TIMER OPERATION

The Neptune subsystem's watchdog timer is provided by the attached ETX COM module. For further information about the watchdog timer function, refer to the specific ETX COM module's User Manual.

11. EEPROM OPERATION

Neptune provides an EEPROM for storage of the address and interrupt level settings for each serial port. The EEPROM is pre-programmed with the factory default values indicated in the following table.

COM Port	Base Address	IRQ #	Protocol
COM3	0x100	5	RS-232
COM4	0x108	5	RS-232
COM5	0x110	5	RS-232
COM6	0x118	5	RS-232

Diamond Systems provides a console application utility, EEPCONF.EXE, which can change the configuration of serial ports COM3-COM6. It is available for download from diamondsystems.com. Source code is also available.

11.1 EEPROM Map and Description

The EEPROM has 256 bytes total, of which the lowest 127 are addressable. EEPROM locations 32–40 are used for storing address and IRQ information for serial ports COM3-COM6. The first four locations (32-35) are used to store the base address values for the four serial ports (COM3-COM6). The second four locations (36-39) are used to store the four interrupt levels (IRQ numbers) for the four serial ports (COM3-COM6). Location 40 is used to store the port protocol for each port. The memory map of the EEPROM is identical to the register map for the addresses and interrupts on Emerald-MM-8P.

EEPROM Address (Register Number)	***Function***
32	COM3 base address (default 0x100)
33	COM4 base address (default 0x108)
34	COM5 base address (default 0x110)
35	COM6 base address (default 0x118)
36	COM3 IRQ No. (default 5)
37	COM4 IRQ No. (default 5)
38	COM5 IRQ No. (default 5)
39	COM6 IRQ No. (default 5)
40	COM3-COM6 Protocol Configuration

The address values stored in EEPROM are the upper 7 bits of the 10-bit serial port address. Each serial port uses 8 registers, so the binary base address of each serial port always ends in 000. To determine the value to store in the EEPROM, truncate the lowest three bits.

Desired base address = 120 Hex = 0 1 0 0 1 0 0 0 0 0

EEPROM value = 0 1 0 0 1 0 0 0 0 0 = 0 1 0 0 1 0 0

These are the 7 uppermost bits of the original base address. This value would be written to the selected port's address location in the EEPROM to program that port for

The IRQ numbers stored in EEPROM are the actual IRQ numbers without any changes. Each port may be programmed for its own IRQ number, or any number of ports may share an IRQ. Not all IRQs are available in all computers. You will need to test for availability and operability of the selected IRQ.

> ***Note:*** *The serial port base addresses must be distinct from each other and must also be distinct from the board's base address. If any serial port's address is programmed to overlap with the board's base address, that port will not be accessible, and the address will have to be reconfigured.*

11.2 How to Use the EEPROM

There are three available EEPROM operations: write data, read data, and reload data.

The write and read operations store data in the EEPROM but have no effect on the board's configuration settings. The reload operation updates the board's configuration settings to match the values stored in the EEPROM.

Note that writing to the board's serial port address and IRQ registers does not cause a write-through to the corresponding EEPROM registers. The user must explicitly write the data to the EEPROM to store these settings for future use when the board is reset or the power is cycled.

The EEPROM contains 256 bytes. However, only locations 0–63 may be accessed.

Only EEPROM addresses 0–17 are used to store data for the configuration of Emerald-MM-8P. The remaining locations are available for customer application use.

11.2.1 EPROM Write Operation

Write data to the EEPROM Data register (Base+21).
Write 6-bit address, and set R/W bit to 1, in the EEPROM Command and Address register (Base+20).
Monitor the BUSY bit in the EEPROM Busy Status register (Base+20) until it is 0.

11.2.2 EEPROM Read Operation

Write 6-bit address, and reset the R/W bit to 0, in the EEPROM Command and Address register (Base+20).
Monitor the BUSY bit in the EEPROM Busy Status register (Base+20) until it is 0.
Read data from the EEPROM Data register (Base+21).

11.2.3 EEPROM Reload Operation

Set the RELOAD bit in the Reload Command register (Base+22) to initiate Reload operation.
Monitor the BUSY bit in the EEPROM Busy Status register (Base+20) until it is 00.

12. DATA ACQUISITION SUBSYSTEM SPECIFICATIONS

12.1 Analog Inputs

- 32 16-bit analog inputs
- Inputs user-configurable as: 32 single-ended, 16 differential, or 16 SE + 8 DI
- Bipolar ranges: ±10V, ±5V, ±2.5V, ±1.25V
- Unipolar ranges: 0-10V, 0-5V, 0-2.5V, 0-1.25V
- Conversion rate: 250,000 samples/second, max.
- FIFO: 1024 samples, programmable threshold
- Accuracy < ±2 LSB, after calibration
- Nonlinearity: ±3LSB, no missing codes
- Input bias current: 100pA max
- Input Impedance: 10^13 ohms
- Protection: ±35V on any analog input without damage
- A/D and D/A calibration: automatic using on-board microcontroller and temp sensor

12.2 Analog Outputs

- 4 12-bit analog outputs
- Output ranges: ±5V, ±10V, 0-5V, 0-10V
- Output current: ±5mA max per channel, 2KΩ min load
- Settling time: 7µS to ±0.01%
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic
- Reset: Reset to zero-scale or mid-scale (jumper selectable)
- Waveform buffer: 1,024 samples

12.3 Programmable Digital I/O Port

- 24 lines with user-programmable direction
- Input logic thresholds :
  - Logic 0: 0.0V min, 0.8V max
  - Logic 1: 2.0V min, 5.0V max
- Input current: ±1µA max
- Output logic thresholds:
  - Logic 0: 0.0V min, 0.33V max
  - Logic 1: 2.4V min, 5.0V max
- Output current:
  - Logic 0: 12mA max per line
  - Logic 1: -4mA max per line

12.4 Optoisolated Inputs and Outputs

- 8 inputs: 5-24V
- 8 outputs: 5-24V

12.5 Counter/Timers

- Clock source: 10MHz on-board clock or external signal
- A/D pacer clock: 24-bit down counter (2 82C54 counters cascaded)
- General purpose: 16-bit down counter (1 82C54 counter)

13. MATING CONNECTOR REFERENCE

The following table lists the on-board connectors and optional interface cables associated with the each of the Neptune baseboard's I/O interfaces and expansion buses.

Note: *Ready-to-use interface cables for all of Neptune's I/O connectors are available through the optional Neptune Cable Kit (Diamond part number C-NPT-KIT). Cable drawings are available on request from Diamond technical support.*

Connector	***Function***	***Board Connector Manufacturer: Part Number***
J1	PC/104-*Plus* ISA bus A,B	EPT: 962-60323-12
J2	PC/104-*Plus* ISA bus C,D	EPT: 962-60203-12
J3	PC/104-*Plus* PCI bus	EPT: 962-60303-12
J4	ETX Utility	Samtec: TMM-110-01-L-D-SM-P
J5	Variable Input Power	Tyco: Electronics 640445-2
J6	Panel I/O Input Power	Samtec: TMM-110-01-L-D-SM-P
J7	Mouse/Keyboard	Samtec: TMM-104-01-L-D-SM-P
J8	VGA	Samtec: TMM-105-01-L-D-SM-P
J10	USB Ports 0-3	Samtec: TMM-110-01-L-D-SM-P
J12	CompactFlash	AVX: 31 5610 050 210 871+
J13	Primary IDE	Sullins: NRPN222MAMP-RC
J14	Primary IDE	Sullins: NRPN222MAMP-RC
J16	LCD-LVDS	JST: BM30B-SRDS-G-TF
J17	LCD Utility	Samtec: TMM-105-01-L-D-SM-P
J18	Audio	Samtec: TMM-105-01-L-D-SM-P
J22	Utility	Samtec: TMM-104-01-L-D-SM-P
J23	HDD Power	Tyco: 640457-4
J24	ETX Ethernet	Samtec: TMM-105-01-L-D-SM-P
J30	Analog Input	Samtec: TMM-120-01-L-D-SM-P
J31	Digital I/O	Samtec: TMM-117-01-L-D-SM-P
J33	Optically isolated I/O	Samtec: TMM-120-01-L-D-SM-P
J34	COM1-4	Samtec: TMM-120-01-L-D-SM-P
J37	COM5-6	Samtec: TMM-110-01-L-D-SM-P
J44	ATX-style input Power	Molex/Waldom: 39-29-6088